# Introduction to Computer Science: Mid-Term Exam 

November 12, 2021. 9:30-11:00

Name (ENG):
Name (CHI): $\qquad$
Student ID:
Instructions (Must Read): Please put down your English name, Chinese name and student ID above.

This paper consists of 50 multiple choice questions.
You need to answer all of them. Each question has only ONE correct answer. Each question carries 2 marks. There is no penalty score if the answer is incorrect.

$$
\text { Score }= \begin{cases}+2 & \text { if the answer is correct } \\ 0 & \text { Otherwise }\end{cases}
$$

For each question, please write down your answer on the left hand side of the question number, by a blue or black ball pen. Writing the answer by pencil is not preferred.

Each question has an option 'None of the above.'. If you have found that options (a), (b), (c) and so on are not correct, you should select this option. Let say a question has five options and option (e) is 'None of the above.'. You should opt (e) if you have found that options (a), (b), (c) and (d) are all incorrect.

Dictionary, calculator, cell phone and computer are not allowed to use during the exam. If you are waiting for an urgent call, please inform Professor John Sum before the examination starts.

Please do not take away this paper. This paper has to be returned for marking.

## SECTION A : Logical Questions

Instructions for Question 1 to Question 10: The questions below are logical questions. In each question, two statements X and Y are given. You have to identify from the following options what is their relation.
(a) Both statements are not true.
(b) Statement X is true. Statement Y is not true.
(c) Statement X is not true. Statement Y is true.
(d) Statement X is true. Statement Y is true. Statement X and Statement Y have no logical implication.
(e) Statement X is true. Statement Y is true. Statement X is a cause of Statement Y .
(f) Statement X is true. Statement Y is true. Statement Y is a cause of Statement X .

## Question 1

X: The teacher of this class is Professor John Sum.
Y: Professor John Sum is a HK-Chinese.

## Question 2

$\mathbf{X}$ : The first assignment was released before the first lecture.
Y: The official email address for assignment submission is pfsum@nchu.edu.tw.

## Question 3

X: In this mid-term exam paper, a student will get 2 marks from a question if the answer of that question is correct.
Y: In this mid-term exam paper, a student will get penalty score -2 marks if the answer of that question is incorrect.

## Question 4

$X$ : Four hundreds years ago, there was no computer.
$Y$ : Four hundreds years ago, there was no information system.

## Question 5

$X$ : There was no electricity in the sixteenth century. $Y$ : There was no communication network in the sixteenth century.

## Question 6

$X$ : Charles Babbage invented the Babbage difference machine in the nineteenth century.
$Y$ : UK made the first commercial electronic computer in the middle of twentieth century.

## Question 7

$X$ : US made atomic bombs in the 1940s.
$Y$ : US had at least one computer in the 1940s.

## Question 8

$X$ : Semiconductor transistor was invented in the 1940s.
$Y$ : The first transistor computer was made in the 1950s.

## Question 9

$X$ : Microsoft Word is an application software running on MacOS only.
$Y$ : Microsoft Word is an application software running on Windows only.

## Question 10

$X$ : Buyer can buy things on eBay.
$Y$ : Buyers are the customers of eBay.

## SECTION B: Normal Questions

## Question 11

Imagine that you are now standing in front of two doors, say X and Y. One of them leads you to heaven and the other leads you to hell. In each door, there is a doorman. Let the doorman standing in front of the door X is A and the doorman standing in front of the door Y is B . For the doormen, it is known that one of them always lies and the other always tells the truth. Besides, the doormen only answer 'Yes' or 'No' to you. For instance, if you ask to a doorman 'the current president of Taiwan is a lady', the liar doorman will answer 'No' and the truth teller doorman will answer 'Yes'.

Now, you can only ask two questions. Which of the following combinations of questions will help you make the right decision on the door to heaven?
(i) The first question is to ask Doorman $\mathrm{X},{ }^{\prime} 1+1=$ 2'. The second question is to ask Doorman Y, 'Door X is the door to heaven'.
(ii) The first question is to ask Doorman X , 'You are a liar'. The second question is to ask Doorman Y , 'Door X is the door to heaven'.
(iii) The first question is to ask Doorman Y, ${ }^{\prime} 1+1=$ 2'. The second question is to ask Doorman X, 'Door Y is the door to heaven'.

## Answer:

(a) (i) and (ii).
(b) (ii) and (iii).
(c) (i) and (iii).
(d) (i), (ii) and (iii).
(e) None of the above.

## Question 12

Imagine that you are now standing in front of two doors, say X and Y. One of them leads you to heaven and the other leads you to hell. In each door, there is a doorman. Let the doorman standing in front of the door X is A and the doorman standing in front of the door Y is B . For the doormen, it is known that one of them always lies and the other always tells the truth. Besides, the doormen only answer 'Yes' or 'No' to you. For instance, if you ask to a doorman 'the current president of Taiwan is a lady', the liar doorman will answer 'No' and the truth teller doorman will answer 'Yes'.

Now, you can only ask one doorman one question. If you have asked the Doorman X the following question: If I ask Doorman Y, 'Door Y will lead me to heaven', Doorman $Y$ will say 'YES'.. Which of the following decision(s) you should made so that you can walk to the door to heaven?
(i) If the Doorman X says 'YES', you walk to the Door X .
(ii) If the Doorman X says 'YES', you walk to the Door Y.
(iii) If the Doorman X says 'NO', you walk to the Door X.
(iv) If the Doorman X says 'NO', you walk to the Door Y.

## Answer:

(a) (i) only.
(b) (ii) only.
(c) (iii) only.
(d) (iv) only.
(e) (i) or (iv) only.
(f) (ii) or (iii) only.

## Diagram for Questions 13-18

The following schematic diagram is for Question 13 to Question 18. It is a circuit consisting of two logic gates.


## Question 13

What are the output values $X$ and $Y$ if A is an XOR gate, B is an AND gate and the input (from left to right) is $101 ?$
(a) $X=0, Y=0$.
(b) $X=0, Y=1$.
(c) $X=1, Y=0$.
(d) $X=1, Y=1$.

## Question 14

What are the output values $X$ and $Y$ if A is an OR gate, B is an OR gate and the input (from left to right) is 111 ?
(a) $X=0, Y=0$.
(b) $X=0, Y=1$.
(c) $X=1, Y=0$.
(d) $X=1, Y=1$.

## Question 15

What are the output values $X$ and $Y$ if A is an AND gate, B is an XOR gate and the input (from left to right) is $101 ?$
(a) $X=0, Y=0$.
(b) $X=0, Y=1$.
(c) $X=1, Y=0$.
(d) $X=1, Y=1$.

## Question 16

What are the output values $X$ and $Y$ if A is an OR gate, $B$ is an NAND gate and the input (from left to right) is $111 ?$
(a) $X=0, Y=0$.
(b) $X=0, Y=1$.
(c) $X=1, Y=0$.
(d) $X=1, Y=1$.

## Question 17

What are the output values $X$ and $Y$ if A is an NAND gate and B is an NAND gate and the input (from left to right) is $111 ?$
(a) $X=0, Y=0$.
(b) $X=0, Y=1$.
(c) $X=1, Y=0$.
(d) $X=1, Y=1$.

## Question 18

What are the output values $X$ and $Y$ if A is an OR gate, B is an AND gate and the input (from left to right) is $1 x 1$ ? Here, ' $x$ ' means that the second input is unknown.
(a) $X=0, Y=0$.
(b) $X=0, Y=1$.
(c) $X=1, Y=0$.
(d) $X=1, Y=1$.

## Question 19

Here are three different sign-magnitude fixed point number presentation formats.
(i) 16-bit format.
sxxxxx.yyyyyyyyyy
(ii) 12-bit format.
sxxxxx.yyyyyy
(iii) 8-bit format.
sxxxxx.yy

Here, $s$ is the sign-bit. $x \cdots x$ is the integer part and $y \cdots y$ is the fractional part. In term of the range of the numbers that can be represented, from the longest to the shortest, which of the following is the correct order?
Answer:
(a) (i) $>$ (ii) $>$ (iii).
(b) (i) $>$ (iii) $>$ (ii).
(c) (ii) $>$ (i) $>$ (iii).
(d) (iii) $>$ (ii) $>$ (i).
(e) None of the above.

## Question 20

Here are three different sign-magnitude fixed point number presentation formats.
(i) 16-bit format.
sxxxxx.yyyyyyyyyy
(ii) 12-bit format.
sxxxxx.yyyyyy
(iii) 8-bit format.

## sxxxxx.yy

Here, $s$ is the sign-bit. $x \cdots x$ is the integer part and $y \cdots y$ is the fractional part. In term of precision error, from the largest to the smallest, which of the following is the correct order?

Answer:
(a) (i) $>$ (ii) $>$ (iii).
(b) (i) $>$ (iii) $>$ (ii).
(c) (ii) $>$ (i) $>$ (iii).
(d) (iii) $>$ (ii) $>$ (i).
(e) None of the above.

## Question 21

Suppose a number represented in the following 16 -bit sign-magnitude fix-point format.
sxxxxxxxxxxx.yyyy
Here, $s$ is the sign-bit. $x \cdots x$ is the integer part and $y \cdots y$ is the fractional part. What is the difference between the third largest number and the fourth largest number?

Answer:
(a) $2^{-2}$.
(b) $2^{-3}$.
(c) $2^{-4}$.
(d) $2^{-5}$.
(e) None of the above.

## Question 22

Which of the following factor(s) will affect the processing time of an instruction?
(i) Clock frequency of a processor.
(ii) Architecture of a processor.
(iii) Micro-program design for an instruction.

## Answer:

(a) (i) and (ii).
(b) (ii) and (iii).
(c) (i) and (iii).
(d) (i), (ii) and (iii).
(e) None of the above.

## Question 23

Which of the following factor(s) will affect the instructions to be included in the set of instructions for a processor?
(i) Clock frequency of a processor.
(ii) Architecture of a processor.
(iii) Micro-program design for an instruction.

## Answer:

(a) (i) and (ii).
(b) (ii) and (iii).
(c) (i) and (iii).
(d) (i), (ii) and (iii).
(e) None of the above.

## Question 24

With reference to the simple processor as shown in the Appendix, Figure 1, suppose that the registers are preset as $R A=1, R B=1, R Z=0, R 1=$ $R 2=R 3=R 4=0$. What will be the contents of the registers $R A$ and $R B$ after the following microinstructions (S1, S2, S3 and S4) have been executed?

S1: $S_{1}=S_{8}=1$. The control signals to other connectors are set to 0 . The signals to all two-way switches are set to 00 .

S2: $S_{14}=01 . \quad S_{12}=S_{15}=10$. The control signals to all connectors are set to 0 . The signals to other two-way switches are set to 00 .

S3: $S_{2}=S_{5}=S_{9}=1$. The control signals to other connectors are set to 0 . The signals to other two-way switches are set to 00 .

S4: $S_{12}=10 . \quad S_{14}=01 . \quad S_{16}=10$. The control signals to other connectors are set to 0 . The signals to other two-way switches are set to 00 .

Answer :
(a) $R A=0, R B=0$.
(b) $R A=0, R B=1$.
(c) $R A=1, R B=0$.
(d) $R A=1, R B=1$.

## Question 25

With reference to the simple processor as shown in the Appendix, Figure 1, suppose that the registers are preset as $R A=1, R B=0, R Z=0, R 1=$ $R 2=R 3=R 4=0$. What will be the contents of the registers $R 1$ and $R 2$ after the following microinstructions (S1, S2, S3 and S4) have been executed?

S1: $S_{1}=S_{8}=1$. The control signals to other connectors are set to 0 . The signals to all two-way switches are set to 00 .

S2: $S_{14}=01 . \quad S_{12}=S_{15}=10$. The control signals to all connectors are set to 0 . The signals to other two-way switches are set to 00 .

S3: $S_{2}=S_{5}=S_{9}=1$. The control signals to other connectors are set to 0 . The signals to other two-way switches are set to 00 .

S4: $S_{12}=10 . \quad S_{14}=01 . \quad S_{16}=10$. The control signals to other connectors are set to 0 . The signals to other two-way switches are set to 00 .

## Answer :

(a) $R 1=0, R 2=0$.
(b) $R 1=0, R 2=1$.
(c) $R 1=1, R 2=0$.
(d) $R 1=1, R 2=1$.

## Question 26

With reference to the simple processor as shown in the Appendix, Figure 1, suppose that the registers are preset as $R A=0, R B=1, R Z=0, R 1=$ $R 2=R 3=R 4=0$. What will be the contents of the registers $R 3$ and $R 4$ after the following microinstructions (S1, S2, S3 and S4) have been executed?

S1: $S_{1}=S_{8}=1$. The control signals to other connectors are set to 0 . The signals to all two-way switches are set to 00 .

S2: $S_{14}=01 . \quad S_{12}=S_{15}=10$. The control signals to all connectors are set to 0 . The signals to other two-way switches are set to 00 .

S3: $S_{2}=S_{5}=S_{9}=1$. The control signals to other connectors are set to 0 . The signals to other two-way switches are set to 00 .

S4: $S_{12}=10 . \quad S_{14}=01 . \quad S_{16}=10$. The control signals to other connectors are set to 0 . The signals to other two-way switches are set to 00 .

## Answer :

(a) $R 3=0, R 4=0$.
(b) $R 3=0, R 4=1$.
(c) $R 3=1, R 4=0$.
(d) $R 3=1, R 4=1$.

## Question 27

With reference to the simple processor as shown in the Appendix, Figure 1, it is assumed that the data in the memory locations $M 1$ and $M 2$ have already been copied to the registers $R A$ and $R B$. What will be the logical operation once the following microinstructions have been executed?

S1: $S_{12}=01$ and $S_{15}=10$. The control signals to other connectors are set to 0 . The signals to all two-way switches are set to 00 .

S2: $S_{12}=10$ and $S_{13}=01$. The control signals to other connectors are set to 0 . The signals to all two-way switches are set to 00 .

S3: $S_{1}=S_{8}=1$. The control signals to other connectors are set to 0 . The signals to all two-way switches are set to 00 .

S4: $S_{12}=10, S_{14}=01$ and $S_{16}=10$. The control signals to all connectors are set to 0 . The signals to other two-way switches are set to 00 .

S5: $S_{13}=10$ and $S_{15}=01$. The control signals to all connectors are set to 0 . The signals to other two-way switches are set to 00 .

S6: $S_{2}=S_{5}=S_{9}=1$. The control signals to other connectors are set to 0 . The signals to other two-way switches are set to 00 .

S7: $S_{12}=10, S_{14}=01$ and $S_{15}=10$. The control signals to other connectors are set to 0 . The signals to other two-way switches are set to 00 .

What of the following instruction have been executed?

## Answer :

(a) $R 1=(\neg R A) R B$ and $R 2=\neg R A$.
(b) $R 1=R A(\neg R B)$ and $R 2=\neg R A$.
(c) $R 1=(\neg R A) R B$ and $R 2=\neg R B$.
(d) $R 1=R A(\neg R B)$ and $R 2=\neg R B$.
(e) None of the above.

## Question 28

With reference to the simple processor as shown in the Appendix, Figure 1, which of the following microprogram(s) can perform the logical operation.

$$
Z=\neg A \oplus \neg B
$$

where $\neg A$ refers to logical NOT A.
(i) 7-Step micro-program.

S1: $S_{1}=S_{8}=1$. Other connectors and switches are set to 'Disconnection' mode.
S2: $S_{14}=01$ and $S_{15}=10$. Other connectors and switches are set to 'Disconnection' mode.
S3: $S_{13}=01$ and $S_{12}=10$. Other connectors and switches are set to 'Disconnection' mode.
S4: $S_{1}=S_{8}=1$. Other connectors and switches are set to 'Disconnection' mode.
S5: $S_{14}=01$ and $S_{13}=10$. Other connectors and switches are set to 'Disconnection' mode.
S6: $S_{15}=01$ and $S_{12}=10$. Other connectors and switches are set to 'Disconnection' mode.
S7: $S_{4}=S_{7}=S_{11}=1$. Other connectors and switches are set to 'Disconnection' mode.
(ii) 8-Step micro-program.

S1: $S_{1}=S_{8}=1$. Other connectors and switches are set to 'Disconnection' mode.
S2: $S_{14}=01$ and $S_{16}=10$. Other connectors and switches are set to 'Disconnection' mode.
S3: $S_{13}=01$ and $S_{12}=10$. Other connectors and switches are set to 'Disconnection' mode.
S4: $S_{1}=S_{8}=1$. Other connectors and switches are set to 'Disconnection' mode.
S5: $S_{14}=01$ and $S_{13}=10$. Other connectors and switches are set to 'Disconnection' mode.
S6: $S_{16}=01$ and $S_{12}=10$. Other connectors and switches are set to 'Disconnection' mode.
S7: $S_{4}=S_{7}=S_{11}=1$. Other connectors and switches are set to 'Disconnection' mode.
S8: $S_{14}=01$ and $S_{15}=10$. Other connectors and switches are set to 'Disconnection' mode.
(iii) One-step micro-program.

S1: $S_{4}=S_{7}=S_{11}=1$. Other connectors and switches are set to 'Disconnection' mode.

## Answer:

(a) (i) and (ii).
(b) (ii) and (iii).
(c) (i) and (iii).
(d) (i), (ii) and (iii).
(e) None of the above.

## Question 29

With reference to the figure as shown in Figure 2, the initial conditions of the processor is set to be following.

$$
\begin{gathered}
S_{1}=S_{2}=S_{3}=0 . S_{12}=S_{13}=S_{14}=00 \\
A 1=A 2=0 . \quad R / W=00 \\
R 1=R 2=R 3=R 4=0 \\
R A=1 . R B=0 . R Z=0
\end{gathered}
$$

What will be the content of $R Z$ and $R 1$ if the following micro-program has been executed?

S1: $\begin{aligned} & S_{1}=S_{2}=S_{3}=1 . \quad S_{12}=S_{13}=S_{14}=00 . \\ & A 1=A 2=0 . R / W=00 .\end{aligned}$

S2: $S_{1}=S_{2}=S_{3}=0 . \quad S_{12}=S_{13}=10 . \quad S_{14}=01$. $A 1=A 2=0 . R / W=00$.

S3: $S_{1}=S_{2}=S_{3}=1 . \quad S_{12}=S_{13}=S_{14}=00$. $A 1=A 2=0 . R / W=00$.

S4: $S_{1}=S_{2}=S_{3}=0 . \quad S_{12}=S_{13}=00 . \quad S_{14}=01$. $A 1=A 2=0 . R / W=10$.

## Answer :

(a) $R Z=0, R 1=0$.
(b) $R Z=0, R 1=1$.
(c) $R Z=1, R 1=0$.
(d) $R Z=1, R 1=1$.

## Question 30

With reference to the figure as shown in Figure 2, the initial conditions of the processor is set to be following.

$$
\begin{gathered}
S_{1}=S_{2}=S_{3}=0 . \quad S_{12}=S_{13}=S_{14}=00 \\
A 1=A 2=0 . \quad R / W=00 \\
R 1=R 2=R 3=R 4=0 \\
R A=0 .
\end{gathered}
$$

What will be the content of $R Z$ and $R 1$ if the following micro-program has been executed?

S1: $S_{1}=S_{2}=S_{3}=1 . \quad S_{12}=S_{13}=S_{14}=00$. $A 1=A 2=0 . R / W=00$.

S2: $S_{1}=S_{2}=S_{3}=0 . \quad S_{12}=01 . \quad S_{13}=00 . \quad S_{14}=$ 01. $A 1=A 2=0 . \quad R / W=00$.

S3: $S_{1}=S_{2}=S_{3}=1 . \quad S_{12}=S_{13}=S_{14}=00$. $A 1=A 2=0 . R / W=00$.

S4: $S_{1}=S_{2}=S_{3}=0 . \quad S_{12}=S_{13}=00 . \quad S_{14}=01$. $A 1=A 2=0 . R / W=10$.

Answer :
(a) $R Z=0, R 1=0$.
(b) $R Z=0, R 1=1$.
(c) $R Z=1, R 1=0$.
(d) $R Z=1, R 1=1$.

## Question 31

With reference to the figure as shown in Figure 2, the initial conditions of the processor is set to be following.

$$
\begin{gathered}
S_{1}=S_{2}=S_{3}=0 . \quad S_{12}=S_{13}=S_{14}=00 \\
A 1=A 2=0 . \quad R / W=00 \\
R 1=R 2=R 3=R 4=0 \\
R A=0 . R B=1 . R Z=0
\end{gathered}
$$

What will be the content of $R 1$ and $R 2$ if the following micro-program has been executed?
S1: $S_{1}=S_{2}=S_{3}=0 . \quad S_{12}=00 . \quad S_{13}=01 . \quad S_{14}=$ 00. $A 1=0 . A 2=0 . R / W=10$.

S2: $S_{1}=S_{2}=S_{3}=0 . \quad S_{12}=01 . \quad S_{13}=10 . \quad S_{14}=$ 00. $A 1=0 . A 2=0 . R / W=00$.

S3: $S_{1}=S_{2}=S_{3}=1 . \quad S_{12}=00 . \quad S_{13}=00 . \quad S_{14}=$ 00. $A 1=0 . A 2=0 . R / W=00$.

S4: $S_{1}=S_{2}=S_{3}=0 . \quad S_{12}=00 . \quad S_{13}=00 . \quad S_{14}=$ 01. $A 1=0 . A 2=1 . R / W=10$.

S5: $S_{1}=S_{2}=S_{3}=0 . \quad S_{12}=10 . \quad S_{13}=10 . \quad S_{14}=$ 00. $A 1=0$. $A 2=0 . R / W=01$.

S6: $S_{1}=S_{2}=S_{3}=1 . \quad S_{12}=00 . \quad S_{13}=00 . \quad S_{14}=$ 00. $A 1=0 . A 2=0 . R / W=00$.

S7: $S_{1}=S_{2}=S_{3}=0 . \quad S_{12}=00 . \quad S_{13}=10 . \quad S_{14}=$ 01. $A 1=0 . A 2=0 . R / W=00$.

S8: $S_{1}=S_{2}=S_{3}=0 . \quad S_{12}=10 . \quad S_{13}=00 . \quad S_{14}=$ 00 . $A 1=0 . A 2=1 . R / W=01$.
S9: $S_{1}=S_{2}=S_{3}=1 . \quad S_{12}=00 . \quad S_{13}=00 . \quad S_{14}=$ 00. $A 1=0$. $A 2=0 . R / W=00$.

S10: $S_{1}=S_{2}=S_{3}=0 . \quad S_{12}=00 . \quad S_{13}=00 . \quad S_{14}=$ 01. $A 1=1 . A 2=0 . R / W=10$.

## Answer :

(a) $R 1=0, R 2=0$.
(b) $R 1=0, R 2=1$.
(c) $R 1=1, R 2=0$.
(d) $R 1=1, R 2=1$.

## Question 32

What will be the content of $R 3$ and $R 4$ if the microprogram in Question 31, with the same initial conditions, has been executed?
Answer :
(a) $R 3=0, R 4=0$.
(b) $R 3=0, R 4=1$.
(c) $R 3=1, R 4=0$.
(d) $R 3=1, R 4=1$.

## Question 33

What will be the content of $R A$ and $R B$ if the microprogram in Question 31, with the same initial conditions, has been executed?

## Answer :

(a) $R A=0, R B=0$.
(b) $R A=0, R B=1$.
(c) $R A=1, R B=0$.
(d) $R A=1, R B=1$.

## Question 34

Here are four memory locations, $M 1, M 2, M 3$ and M4. Refer to the artificial CPU and its commands, what will be the content of $M 4$ if the following commands are executed?

DEF M1 3
DEF M2 5
DEF M3 2

MOV IA M1
MOV IB M2
ADD IA IB
MOV IA OUT
MOV IB M3
MUL IA IB
MOV M4 OUT

Answer :
(a) 16 .
(b) 21 .
(c) 25 .
(d) 30 .
(e) None of the above.

## Question 35

Here are four memory locations, M1, M2, M3 and M4. Refer to the artificial CPU and its commands, what will be the content of M4 if the following commands are executed?

DEF M1 3
DEF M2 5
DEF MЗ 2

MOV IA M1
MOV IB M2
ADD IA IB
ADD IA IB
MOV IA OUT

MOV IB M3
MUL IA IB
MOV M4 OUT

## Answer :

(a) 16 .
(b) 21 .
(c) 26 .
(d) 32 .
(e) None of the above.

## Question 36

Here are four memory locations, M1, M2, M3 and M4. Refer to the artificial CPU and its commands, what will be the contents of the registers $I B$ and $O U T$ if the following commands are executed?

```
DEF M1 3
DEF M2 5
DEF M3 2
MOV IA M1
MOV IB M2
ADD IA IB
MOV IA OUT
MOV IB M3
ADD IA IB
MOV M4 OUT
```


## Answer :

(a) $I B=0$ and $O U T=0$.
(b) $I B=2$ and $O U T=0$.
(c) $I B=0$ and $O U T=10$.
(d) $I B=2$ and $O U T=10$.
(e) None of the above.

## Question 37

What will be the content of $M 4$ if the following program segment is executed?

DEF M1 16
DEF M2 22
DEF M3 10
MOV IA M1
MOV IB M2
CMP IA IB
MOV M4 OUT
MOV IA M2
MOV IB M3

CMP IA IB
MOV IA OUT
MOV IB M4
ADD IA IB
MOV M4 OUT

## Answer :

(a) 28 .
(b) 30 .
(c) 32 .
(d) 34 .
(e) None of the above.

## Question 38

Find the value of M3 after the following program segment has been executed.
-----------
DEF M1 13
DEF M2 12

MOV IA M1
SHL IA 00000100
MOV IA OUT
MOV IB M2
ADD IA IB
MOV M3 OUT

## Answer :

(a) $M 3=25$.
(b) $M 3=38$.
(c) $M 3=51$.
(d) $M 3=64$.
(e) None of the above.

## Question 39

Refer to the artificial CPU and its commands, what will be the content of M4 if the following commands are executed?

```
DEF M1 2
DEF M2 2
DEF M3 5
MOV IA M1
IF IA == 0
    MOV IA M2
    SHL IA 00000100
    MOV IA OUT
DEF M2 }
```


## Answer :

(a) 7 .
(b) 9 .
(c) 13 .
(d) 21 .
(e) None of the above.

## Question 41

Given that there are five memories M1, M2, M3, M4 and M5. Here is the program segment to instruct the circuit.

MOV IA M1
MOV IB M2
MUL IA IB
MOV IA OUT
MOV IB M3
MUL IA IB
MOV IA OUT
MOV IB M4
SUB IA IB
MOV M5 OUT
----------------
Which of the following mathematical equation is identical to the operation of the following program segment?

Answer :
(a) $M 5=M 4-M 1 \times M 2 \times M 3$.
(b) $M 5=M 4-(M 1+M 2) \times M 3$
(c) $M 5=M 1 \times M 2 \times M 3-M 4$.
(d) $M 5=(M 1+M 2) \times M 3-M 4$.
(e) None of the above.

## Question 42

Given that there are two memories $M 1$ and $M 2$. Here is the program segment to instruct the circuit.

```
MOV IA M1
MOV IB M2
SHL IA 00000100
MOV IA OUT
SHL IB 00000101
MOV IB OUT
ADD IA IB
MOV IB OUT
MOV IA M1
ADD IA IB
MOV M2 OUT
-
```

Which of the following mathematical equation is identical to the operation of the following program segment?

## Answer :

(a) $M 2=3 \times M 1$.
(b) $M 2=5 \times M 1$.
(c) $M 2=7 \times M 1$.
(d) $M 2=9 \times M 1$.
(e) None of the above.

## Question 43

Given that there are four memory slots $M 1, M 2, M 3$ and M4. Here is the program segment to instruct the circuit.

MOV IA M1
MOV IB M2
SHL IA 00000100
MOV IA OUT
SHL IB 00000010
MOV IB OUT
ADD IA IB
MOV IB OUT
MOV IA M3
ADD IA IB
MOV M4 OUT

Which of the following mathematical equation is identical to the operation of the following program segment?

Answer :
(a) $M 4=2 \times(2 \times M 1+M 2)+M 3$.
(b) $M 4=2 \times(M 1+2 \times M 2)+M 3$.
(c) $M 4=M 1+2 \times(M 2+2 \times M 3)$.
(d) $M 4=7 \times(M 1+M 2+M 3)$.
(e) None of the above.

## Question 44

Which of the following task(s) is(are) the job(s) of an operating system?
(i) File management.
(ii) Memory management.
(iii) Process management.

## Answer:

(a) (i) and (ii).
(b) (ii) and (iii).
(c) (i) and (iii).
(d) (i), (ii) and (iii).
(e) None of the above.

## Question 45

Which of the following statement(s) is(are) true?
(i) Once a computer has been power on, the first instruction the processor (CPU) has to execute is got from BIOS.
(ii) BIOS is a random access memory (RAM).
(iii) Once a computer has been power off, the contents in the BIOS will be gone.

## Answer:

(a) (i) and (ii).
(b) (ii) and (iii).
(c) (i) and (iii).
(d) (i), (ii) and (iii).
(e) None of the above.

## Question 46

Which of the following system(s) is(are) an operating system?
(i) Apple iOS for iPhone.
(ii) Apple MacOS for Macintosh.
(iii) Microsoft Windows for Acer notebook computers.

## Answer:

(a) (i) and (ii).
(b) (ii) and (iii).
(c) (i) and (iii).
(d) (i), (ii) and (iii).
(e) None of the above.

## Question 47

Which of the following system(s) is(are) an application software or application system?
(i) FB Messenger APP for Android.
(ii) LINE for Android.
(iii) Whatsapp for iOS.

## Answer:

(a) (i) and (ii).
(b) (ii) and (iii).
(c) (i) and (iii).
(d) (i), (ii) and (iii).
(e) None of the above.

## Question 48

Which of the following method(s) is(are) for a user to control an operating system?
(i) Text command.
(ii) GUI-based command.
(iii) Voice command.

## Answer:

(a) (i) and (ii).
(b) (ii) and (iii).
(c) (i) and (iii).
(d) (i), (ii) and (iii).
(e) None of the above.

## Question 49

In a computer lab, you have found that a computer has no response to any typing. What of the following action(s) you cannot do?
(i) Plug out the power cord and reconnect it. So that, the computer will be restarted.
(ii) Press the power on button to re-start the computer.
(iii) Press CTRL-ALT-DEL. If the task manager window appears, select 'restart the computer' option.

## Answer:

(a) (i) and (ii).
(b) (ii) and (iii).
(c) (i) and (iii).
(d) (i), (ii) and (iii).
(e) None of the above.

## Question 50

A powerful computer could be set for multiple-user access. Let say a computer has been set to be accessible to three users John, Mary and Tom. The access right of a file is managed by the user self. The following table depicts the access right controls of three files X, Y and Z.

| File | John | Mary | Tom |
| :---: | :---: | :---: | :---: |
| X | RWD | R | - |
| Y | - | RWD | - |
| Z | - | R | RWD |

Clearly, John and Tom do not want their files to be readable to each other. Note that some settings depicted in the above table are set by the file owner. Some settings are default setting. Even the file owner does not know the setting.

In accordance with the above setting, which of the following leakage(s) could/will happen?
(i) The content of file X could be leaked to Tom.
(ii) The content of file Y will be leaked to both John and Tom.
(iii) The content of file Z could be leaked to John.

## Answer:

(a) (i) and (ii).
(b) (ii) and (iii).
(c) (i) and (iii).
(d) (i), (ii) and (iii).
(e) None of the above.

## APPENDIX

In this appendix, it includes the information about a simple processor, an artificial CPU and the source codes of five programs. Please read them carefully!

## A. Processor with 4 Logic Gates

A simple processor, with a sector of four logic gates and a sector of four registers, shown in Figure 1. Each register is associated with a two-way switch. The signals to be fed to the switch and the corresponding actions are depicted in the following table.

| $S_{i}$ | Action |
| :---: | :---: |
| 00 | Disconnect. |
| 01 | Read from register. |
| 10 | Write to register. |

For each connector, its control signal is either ' 0 ' (for disconnection) and ' 1 ' (for connection).

$$
\text { Connection }= \begin{cases}\text { Connect } & \text { if } S_{i}=1 \\ \text { Disconnect } & \text { if } S_{i}=0\end{cases}
$$



Two-Way Switches: Disconnected (00); Down (01), Up (10).

$$
\left(S_{12}, S_{13}, S_{14}, S_{15}, S_{16}, S_{17}, S_{18}\right)
$$

Connectors: Disconnected (0), Connected (1).
$\left(S_{1}, S_{2}, S_{3}, S_{4}, S_{5}, S_{6}, S_{7}, S_{8}, S_{9}, S_{10}, S_{11}\right)$
Figure 1: A processor with four logic gates. Switches $S_{1}$ to $S_{11}$ are simple switches (i.e. connectors). $S_{12}$ to $S_{18}$ are two-way switches.

## B. Processor with a NAND Gate

Figure 2 shows a simple processor with single NAND gate inside. Switches $S_{1}, S_{2}$ and $S_{3}$ are simple
switches (i.e. connectors). $S_{12}, S_{13}$ and $S_{14}$ are twoway switches. The signals sending to $A 1, A 2$ and $R / W$ together with the corresponding actions are depicted in the following table.

| $A 1$ | $A 2$ | $R / W$ | Action |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 01 | Read data from $R 1$ |
| 0 | 1 | 01 | Read data from $R 2$ |
| 1 | 0 | 01 | Read data from $R 3$ |
| 1 | 1 | 01 | Read data from $R 4$ |
| 0 | 0 | 10 | Write data to $R 1$ |
| 0 | 1 | 10 | Write data to $R 2$ |
| 1 | 0 | 10 | Write data to $R 3$ |
| 1 | 1 | 10 | Write data to $R 4$ |
| x | x | 00 | Disconnection |



Figure 2: A processor with single NAND gate.

## C. Artificial CPU

Below is a simple circuit. It consists of a memory with 16 memory spaces (from M1 to M16), an ALU block, 2 input registers (IA and IB) and one output register (OUT). M1 to M16, IA, IB and OUT are all 8 bits long. Numbers are represented in 2's compliment format.


Eleven commands (MOV, ADD, SUB, MUL, DIV, CMP, SHL, SHR, DEF, MSK and IF) are provided for instructing the above circuit. The syntax and the descriptions of these commands are depicted in Table 1.

Table 1: Commands for using the CPU.

| Syntax | Description |
| :--- | :--- |
| MOV X Y | Copy the content of Y to X |
| ADD X Y | $O U T=X+Y$. |
| SUB X Y | $O U T=X-Y$. |
| MUL X Y | $O U T=X \times Y$. |
| DIV X Y | $O U T=X / Y$. |
| CMP X Y | $O U T=b_{1} b_{2} b_{3} b_{4} b_{5} b_{6} b_{7} b_{8}$. |
|  | $b_{i}=0$ if $X_{i}=Y_{i}$. |
| SHL X Y | $b_{i}=1$ if $X_{i} \neq Y_{i}$. |
|  | $O U T$ is the content of X |
| shifting left Y bits. |  |
| SHR X Y | $O U T$ is the content of X |
|  | Shifting right Y bits. |
| DEF X N | Define X as the number N. |
| MSK X M | Mask the value of X by M. |
| IF ELSE | Condition statement. |

## D. Notes on CPU Commands

1. For the "CMP" command, if $X=0110$ and $Y=$ $1101, O U T=1011$.
2. For "SHL" and "SHR" commands, the content of $Y$ can only be one of the following.

| $Y$ | Meaning |
| :--- | :--- |
| 10000000 | (Shift 7 bits) |
| 01000000 | (Shift 6 bits) |
| 00100000 | (Shift 5 bits) |
| 00010000 | (Shift 4 bits) |
| 00001000 | (Shift 3 bits) |
| 00000100 | (Shift 2 bits) |
| 00000010 | (Shift 1 bits) |
| 00000001 | (No shift) |

For example, if

$$
X=00011000, Y=00000100,
$$

the OUT of "SHL X Y" is 01100000 and the OUT of "SHR X Y" is 00000110.
3. For the "DEF" command, $N$ must be a number in decimal form. $X$ can only be a memory location. "DEF" command is not applicable for assigning values to a register. It is used to assign a value to a memory location. For example, "DEF M1 12 " means that memory location

M1 will be assigned with a value 12. Therefore, $M 1=00001100$.
4. For the "MSK" command, it is used for masking a register (either IA or IB) by the mask $M$ (in binary). The mask must be 8 bits long.
Suppose that the content of $I A$ and $M$ are defined as follows :

$$
I A=01001001, M=11110000
$$

Then, the output $O U T$ will be " 01000000 ". The last four bits are masked. Here is an example.

```
DEF M1 45
MOV IA M1
MSK IA 00001111
MOV M2 OUT
```

Initially, $M 1$ is assigned with value 45 . In binary form, the content reads "00101101". Thus, the output OUT is " 00001101 ".
5. The "IF-ELSE" command is an advanced level command. It is for conditional statement. Once it is executed, the CPU will performs multiple steps in order to make it works. You do not need to know the detail how it works. In term of its usage, it is simple. Here is an example.

```
DEF M1 1
DEF M2 2
DEF M3 1
MOV IA M1
IF IA == 0
    MOV IA M2
    MOV IB M3
    ADD IA IB
    MOV M4 OUT
ELSE
    MOV IA M1
    ADD IB M2
    MOV M4 OUT
ENDIF
```

Command "IF" checks if the content of IA is identical to " 0 ". If it is, it will perform $M 2+M 3$ and output the result to M4. Otherwise, it will perform $M 1+M 2$ and output the result to $M 4$.

DEF M3 1
MOV IA M1
IF $\mathrm{IA}==0$
MOV IA M2
MOV IB M3
ADD IA IB
MOV M4 OUT
ENDIF

In this example, the CPU performs $M 2+M 3$ only if $I A$ is zero. Otherwise, it performs nothing.
6. For the "IF-ELSE" command, the following conditions are allowed for you to define. Here NUM must be stated in decimal form but not in binary.

```
IA == NUM
IA > NUM
IA >= NUM
IA < NUM
IA <= NUM
```

```
DEF M1 1
DEF M2 2
```

