

Introduction to Computer Science: Mid-Term Exam

November 4, 2022. 9:30 - 11:00

Name: _____

Student ID: _____

Instructions (Must Read):

- (1) Please fill in your name and student ID.
- (2) This paper consists of multiple choice questions. You need to answer all of them. Each question has only ONE correct answer. Each question carries 2 marks.
- (3) The questions are divided into two sections. Section A consists of 15 logical questions. Please follow the instructions described in the section to answer the questions. Section B consists of 35 questions.
- (4) For each question, please write down your answer (i.e. the option) on the left hand side of its question number, by a blue or black ball pen. Writing the answer by pencil is not preferred.
- (5) Some questions have an option 'None of the above.'. If you have found that options (a), (b), (c) and so on are not correct, you should select this option. Let say a question has five options and option (e) is 'None of the above.'. You should opt (e) if you have found that options (a), (b), (c) and (d) are all incorrect.
- (6) Dictionary, cell phone, computer, pad and the devices which are able to connect to the Internet are not allowed to use during the exam. If you are waiting for an urgent call, please inform Professor John Sum before the examination starts.

Please do not take away this paper. This paper has to be returned for marking.

SECTION A : Logical Questions

Instructions for Question 1 to Question 15:

The questions below are logical questions. In each question, two statements X and Y are given. You have to identify from the following options what is their relation.

- (a) Both statements are not true.
- (b) Statement X is true. Statement Y is not true.
- (c) Statement X is not true. Statement Y is true.
- (d) Statement X is true. Statement Y is true. Statement X and Statement Y have no logical implication.
- (e) Statement X is true. Statement Y is true. Statement X is a cause of Statement Y.
- (f) Statement X is true. Statement Y is true. Statement Y is a cause of Statement X.

Question 1

X: The file of an operating system is an executable file. Its file extension is *.exe*.

Y: All PDF file is an executable file. The file extension of a PDF file is *.pdf*.

Question 2

X: Windows operating system (OS) is able to handle multitasking.

Y: While the Windows OS has been initialized, it is able to invoke Chrome for accessing webpages and concurrently invoke MS WORD for document editing.

Question 3

X: Once an application software has been invoked, the operating system will assign a process ID for it.

Y: Once an application software has been invoked, the operating system will allocate working memory space for it.

Question 4

X: Once a computer has been power on, the first instruction to be executed by a CPU is got from the main memory, either in a harddrive or solid state drive.

Y: Once a computer has been power on, the first instruction to be executed by a CPU is got from the BIOS.

Question 5

X: The design of an operating system is dependent on the set of instructions provided by the CPU to be used in a computer.

Y: The MacOS designed for all Intel processor-based Mac series computers has to be re-designed for all Apple M1 processor-based Mac series computers.

Question 6:

X: During system initialization, the operating system will invoke all device drivers to be running as background processes and assign with them distinct process IDs.

Y: A printer cannot be used if its device driver has not been installed and invoked by the operating system.

Question 7

X: An information system is a set of interrelated components responsible for collecting, storing, processing and distributing information within an organization to support decision making.

Y: Without computer and networking technologies, it is unable to have an information system in an organization.

Question 8

X: Reading/Writing a data from/to the main memory is the work to be executed by the CPU.

Y: Reading an instruction from the main memory is the work to be executed by the CPU.

Question 9

X: The name of the professor who teaches this class is called Janet Chang.

Y: Professor Janet Chang is a Hong Kong born Chinese.

Question 10

X: Students are allowed to bring with their cell phones, notebook computer and pads in the classroom.

Y: Students can freely access any webpage over the Internet during the lectures.

Question 11

X: There was no computer in the nineteenth century.

Y: Vacuum tube had not been invented in the nineteenth century.

Question 12

X: We are now able to send a letter to a friend via the Internet to his/her email account.

Y: In the nineteenth century, it was unable to send any letter to any friend.

Question 13

X: Suppose that you have subscribed the voice service from a local Taiwan telecommunication firm, your cell phone will automatically connected to the 4G telecommunication network every time when you have made a phone call to your friend by dialing his/her telephone number.

Y: The 4G telecommunication network is able to support both voice service and data service.

Question 14

It is assumed that a number is encoded as a 16-bit fixed point format as follows :

sxxxx.ffffffffff

where the leading bit *s* is the sign bit, the subsequent 5 bits *xxxxx* is for the integer part while the last 10 bits is for the fractional part. The rounding method is round-by-chop. The following example shows a procedure how a decimal number +3.1 is converted to the above 16-bit fixed-point format.

=====
Number conversion with round-by-chop.
=====

Step 1: Convert +3.1 to binary.
3.1 = 11.0001100110011

Step 2: Normalize to 5 integer bits.
3.1 = 00011.0001100110011

Step 3: Add sign bit.
+3.1 = 000011.0001100110011

Step 4: Chop the tail bits.
+3.1 = 000011.0001100110

=====

X: Converting a decimal number to the above fixed point format by using round-by-chop requires fewer steps than using round-to-nearest rounding method.

Y: The maximum rounding error of a decimal number being converted to the above fixed point format by using round-by-chop smaller than the maximum rounding error of a decimal number being converted to the above fixed point format by using round-to-nearest rounding method.

Question 15

X: Today, multiple central processing units can be embedded in a single chip. The chip with multiple CPUs inside is usually called multi-core processor. Each core in the processor corresponds to one CPU.

Y: Today, the advancement of the fabrication technology is able to make a logic gate with size in nanometer (nm) scale.

SECTION B: Normal Questions

Question 16

Imagine that you are now standing in front of two doors, say X and Y. One of them leads you to heaven and the other leads you to hell. In each door, there is a doorman. Let the doorman standing in front of the door X is A and the doorman standing in front of the door Y is B. For the doormen, it is known that one of them always lies and the other always tells the truth. Besides, the doormen only answer 'Yes' or 'No' to you. For instance, if you ask to a doorman 'the current president of Taiwan is a lady', the liar doorman will answer 'No' and the truth teller doorman will answer 'Yes'.

Now, you can only ask two questions. Which of the following combinations of questions will help you make the right decision on the door to heaven?

- (i) The first question is to ask Doorman X, ' $1 + 1 = 2$ '. The second question is to ask Doorman Y, 'Door X is the door to heaven'.
- (ii) The first question is to ask Doorman X, 'You are a liar'. The second question is to ask Doorman Y, 'Door X is the door to heaven'.
- (iii) The first question is to ask Doorman Y, ' $1 + 1 = 2$ '. The second question is to ask Doorman X, 'Door Y is the door to heaven'.

Answer:

- (a) (i) and (ii).
- (b) (ii) and (iii).
- (c) (i) and (iii).

(d) (i), (ii) and (iii).

(e) None of the above.

Question 17

Imagine that you are now standing in front of two doors, say X and Y. One of them leads you to heaven and the other leads you to hell. In each door, there is a doorman. Let the doorman standing in front of the door X is A and the doorman standing in front of the door Y is B. For the doormen, it is known that one of them always lies and the other always tells the truth. Besides, the doormen only answer 'Yes' or 'No' to you. For instance, if you ask to a doorman 'the current president of Taiwan is a lady', the liar doorman will answer 'No' and the truth teller doorman will answer 'Yes'.

Now, you can only ask one doorman one question. If you have asked the Doorman X the following question: *If I ask Doorman Y, 'Door Y will lead me to heaven', Doorman Y will say 'YES'.* Which of the following decision(s) you should made so that you can walk to the door to heaven?

- (i) If the Doorman X says 'YES', you walk to the Door X.
- (ii) If the Doorman X says 'YES', you walk to the Door Y.
- (iii) If the Doorman X says 'NO', you walk to the Door X.
- (iv) If the Doorman X says 'NO', you walk to the Door Y.

Answer:

- (a) (i) only.
- (b) (ii) only.
- (c) (iii) only.
- (d) (iv) only.
- (e) (i) or (iv) only.
- (f) (ii) or (iii) only.

Question 18

In a desktop computer or a notebook computer, which of the following factor(s) is(are) the possible reason(s) why an operating system (OS) of a notebook computer is not stored in the BIOS?

- (i) The memory size of an operating system is too big.
- (ii) The computer is unlikely to install and run the OS other than the hardwired OS.

- (iii) Even if the emulator of a new OS has been installed and running, the performance of the computer in running an application software on top of the new OS will be degraded because the emulator of the new OS cannot direct interact with the hardware. The emulator needs to interface to the hardwired OS for interacting the hardware.

Answers:

- (a) (i) and (ii).
 (b) (ii) and (iii).
 (c) (i) and (iii).
 (d) (i), (ii) and (iii).
 (e) None of the above.

Table of Question 19-22

The following table depicts the meaning of the notations in an equation performing logical operation.

Logical Operations	Descriptions
$\neg A$	NOT A
AB	AND A B
$A + B$	OR A B
$A \oplus B$	XOR A B
$\neg(AB)$	NAND A B

Question 19

Which of the following truth table is for the logical operation given below?

$$Z = (\neg A) \oplus (\neg B).$$

Answer:

(a)

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

(b)

A	B	Z
0	0	1
0	1	0
1	0	1
1	1	1

(c)

A	B	Z
0	0	1
0	1	1
1	0	0
1	1	1

(d)

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

- (e) None of the above.

Question 20

Which of the following truth table is for the logical operation given below?

$$Z = A \oplus (\neg B).$$

Answer:

(a)

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

(b)

A	B	Z
0	0	1
0	1	0
1	0	1
1	1	1

(c)

A	B	Z
0	0	1
0	1	1
1	0	0
1	1	1

(d)

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

- (e) None of the above.

Question 21

Which of the following truth table is for the logical operation given below?

$$Z = (A \oplus B) + B.$$

Answer:

(a)

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

A	B	Z
0	0	1
0	1	0
1	0	1
1	1	1

(b)

A	B	Z
0	0	1
0	1	1
1	0	0
1	1	1

(c)

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

(d)

(e) None of the above.

Question 22

Which of the following truth table is for the logical operation given below?

$$Z = (\neg A) + (A \oplus B).$$

Answer:

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

(a)

A	B	Z
0	0	1
0	1	0
1	0	1
1	1	1

(b)

A	B	Z
0	0	1
0	1	1
1	0	0
1	1	1

(c)

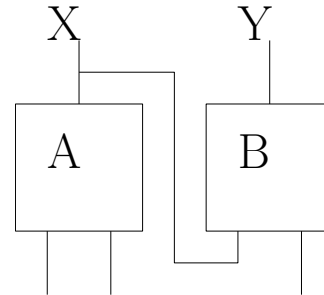
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

(d)

(e) None of the above.

Diagram for Questions 23-28

The following schematic diagram is for Question 23 to Question 28. It is a circuit consisting of two logic gates.



Question 23

What are the output values X and Y if A is an XOR gate, B is an AND gate and the input (from left to right) is 101?

(a) $X = 0, Y = 0.$

(b) $X = 0, Y = 1.$

(c) $X = 1, Y = 0.$

(d) $X = 1, Y = 1.$

Question 24

What are the output values X and Y if A is an OR gate, B is an OR gate and the input (from left to right) is 111?

(a) $X = 0, Y = 0.$

(b) $X = 0, Y = 1.$

(c) $X = 1, Y = 0.$

(d) $X = 1, Y = 1.$

Question 25

What are the output values X and Y if A is an AND gate, B is an XOR gate and the input (from left to right) is 101?

(a) $X = 0, Y = 0.$

(b) $X = 0, Y = 1.$

(c) $X = 1, Y = 0.$

(d) $X = 1, Y = 1.$

Question 26

What are the output values X and Y if A is an OR gate, B is an NAND gate and the input (from left to right) is 111?

- (a) $X = 0, Y = 0$.
- (b) $X = 0, Y = 1$.
- (c) $X = 1, Y = 0$.
- (d) $X = 1, Y = 1$.

Question 27

What are the output values X and Y if A is an OR gate, B is an XOR gate and the input (from left to right) is 1x1? Here, 'x' means that the second input is unknown.

- (a) $X = 0, Y = 0$.
- (b) $X = 0, Y = 1$.
- (c) $X = 1, Y = 0$.
- (d) $X = 1, Y = 1$.

Question 28

What are the output values X and Y if A is an OR gate, B is an OR gate and the input (from left to right) is 1xy? Here, 'x' (resp. 'y') means that the second (resp. third) input is unknown.

- (a) $X = 0, Y = 0$.
- (b) $X = 0, Y = 1$.
- (c) $X = 1, Y = 0$.
- (d) $X = 1, Y = 1$.

Question 29

Here are three different sign-magnitude fixed point number presentation formats.

- (i) 16-bit format.

sxxx.yyyyyyyyyyyy

- (ii) 16-bit format.

sxxxx.yyyyyyyyyyyy

- (iii) 16-bit format.

sxxxxx.yyyyyyyyyyyy

Here, s is the sign-bit. $x \cdots x$ is the integer part and $y \cdots y$ is the fractional part. In term of the range of the numbers that can be represented, from the longest to the shortest, which of the following is the correct order?

Answer:

- (a) (i) > (ii) > (iii).
- (b) (i) > (iii) > (ii).
- (c) (ii) > (i) > (iii).
- (d) (iii) > (ii) > (i).
- (e) None of the above.

Question 30

Here are three different sign-magnitude fixed point number presentation formats.

- (i) 16-bit format.

sxxx.yyyyyyyyyyyy

- (ii) 16-bit format.

sxxxx.yyyyyyyyyyyy

- (iii) 16-bit format.

sxxxxx.yyyyyyyyyyyy

Here, s is the sign-bit. $x \cdots x$ is the integer part and $y \cdots y$ is the fractional part. The rounding method of the above formats is round-by-chop. In term of the maximum rounding error, from the largest to the smallest, which of the following order is the correct?

Answer:

- (a) (i) > (ii) > (iii).
- (b) (i) > (iii) > (ii).
- (c) (ii) > (i) > (iii).
- (d) (iii) > (ii) > (i).
- (e) None of the above.

Question 31

Here are three different sign-magnitude fixed point number presentation formats.

- (i) 16-bit format.

sxxx.yyyyyyyyyyyy

- (ii) 16-bit format.

sxxxx.yyyyyyyyyyy

(iii) 16-bit format.

sxxxxx.yyyyyyyyyyy

Here, s is the sign-bit. $x \dots x$ is the integer part and $y \dots y$ is the fractional part. The rounding method of the above formats is round-to-nearest. In term of the maximum rounding error, from the largest to the smallest, which of the following order is the correct?

Answer:

- (a) (i) > (ii) > (iii).
- (b) (i) > (iii) > (ii).
- (c) (ii) > (i) > (iii).
- (d) (iii) > (ii) > (i).
- (e) None of the above.

Question 32

Suppose a number represented in the following 16-bit sign-magnitude fix-point format.

sxxxxxxxxxxxx.yyyy

Here, s is the sign-bit. $x \dots x$ is the integer part and $y \dots y$ is the fractional part. What is the difference between any two consecutive numbers?

Answer:

- (a) 2^{-2} .
- (b) 2^{-3} .
- (c) 2^{-4} .
- (d) 2^{-5} .
- (e) None of the above.

Question 33

In term of the maximum rounding error (MRE), which of the following format(s) has(have) the same MRE?

(i) Round-by-chop is applied to the format below.

sxxxxxxxxxxxx.yyyy

(ii) Round-by-chop is applied to the format below.

sxxxxxxx.yyyy

(iii) Round-to-nearest is applied to the format below.

sxxxxxxxxxxx.yyy

Answers:

- (a) (i) and (ii).
- (b) (ii) and (iii).
- (c) (i) and (iii).
- (d) (i), (ii) and (iii).
- (e) None of the above.

Question 34

Which of the following factor(s) will affect the processing time of an instruction?

- (i) Clock frequency of a processor.
- (ii) Architecture of a processor.
- (iii) Micro-program design for an instruction.

Answer:

- (a) (i) and (ii).
- (b) (ii) and (iii).
- (c) (i) and (iii).
- (d) (i), (ii) and (iii).
- (e) None of the above.

Question 35

Figure 1 shows a logic circuit with four full adders. If $A_3A_2A_1A_0 = 0101$, what is the output $Z_4Z_3Z_2Z_1Z_0$?

Answer:

- (a) $Z = 1010$.
- (b) $Z = 1011$.
- (c) $Z = 01010$.
- (d) $Z = 01011$.
- (e) None of the above.

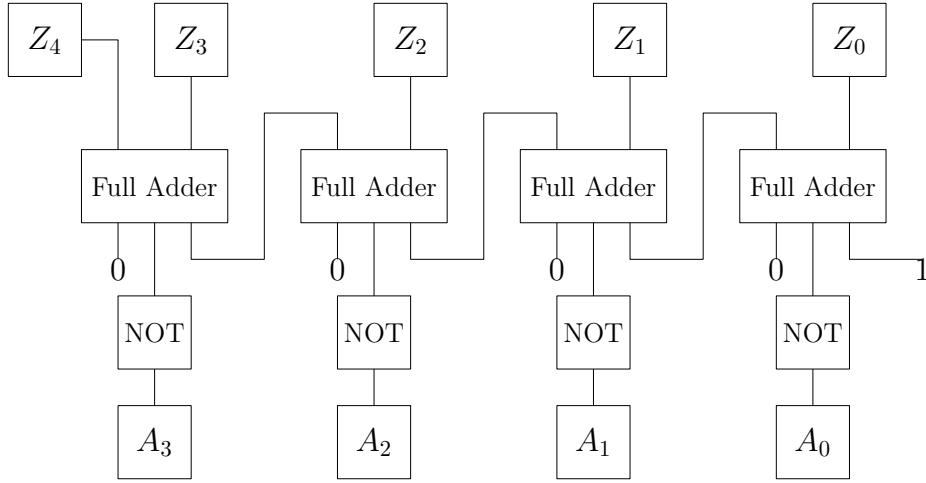


Figure 1: A logic circuit with four full adders. The rightmost input of the rightmost full adder is always connected to logical '1'.

Question 36

With reference to the simple processor as shown in the Appendix, Figure 2, suppose that the registers are preset as $RA = 1, RB = 0, RZ = 0, R1 = R2 = R3 = R4 = 1$. What will be the contents of the registers RA and RB after the following micro-instructions (S1, S2, S3 and S4) have been executed?

- S1: $S_1 = S_8 = 1$. The control signals to other connectors are set to 0. The signals to all two-way switches are set to 00.
- S2: $S_{14} = 01, S_{12} = S_{15} = 10$. The control signals to all connectors are set to 0. The signals to other two-way switches are set to 00.
- S3: $S_2 = S_5 = S_9 = 1$. The control signals to other connectors are set to 0. The signals to other two-way switches are set to 00.
- S4: $S_{12} = 10, S_{14} = 01, S_{16} = 10$. The control signals to other connectors are set to 0. The signals to other two-way switches are set to 00.

Answer :

- (a) $RA = 0, RB = 0$.
- (b) $RA = 0, RB = 1$.
- (c) $RA = 1, RB = 0$.
- (d) $RA = 1, RB = 1$.

Question 37

With reference to the simple processor as shown in the Appendix, Figure 2, suppose that the registers are preset as $RA = 1, RB = 0, RZ = 0, R1 =$

$R2 = R3 = R4 = 1$. What will be the contents of the registers $R1$ and $R2$ after the following micro-instructions (S1, S2, S3 and S4) have been executed?

- S1: $S_1 = S_8 = 1$. The control signals to other connectors are set to 0. The signals to all two-way switches are set to 00.
- S2: $S_{14} = 01, S_{12} = S_{15} = 10$. The control signals to all connectors are set to 0. The signals to other two-way switches are set to 00.
- S3: $S_2 = S_5 = S_9 = 1$. The control signals to other connectors are set to 0. The signals to other two-way switches are set to 00.
- S4: $S_{12} = 10, S_{14} = 01, S_{16} = 10$. The control signals to other connectors are set to 0. The signals to other two-way switches are set to 00.

Answer :

- (a) $R1 = 0, R2 = 0$.
- (b) $R1 = 0, R2 = 1$.
- (c) $R1 = 1, R2 = 0$.
- (d) $R1 = 1, R2 = 1$.

Question 38

With reference to the simple processor as shown in the Appendix, Figure 2, suppose that the registers are preset as $RA = 1, RB = 0, RZ = 0, R1 = R2 = R3 = R4 = 1$. What will be the contents of the registers $R3$ and $R4$ after the following micro-instructions (S1, S2, S3 and S4) have been executed?

S1: $S_1 = S_8 = 1$. The control signals to other connectors are set to 0. The signals to all two-way switches are set to 00.

S2: $S_{14} = 01$. $S_{12} = S_{15} = 10$. The control signals to all connectors are set to 0. The signals to other two-way switches are set to 00.

S3: $S_2 = S_5 = S_9 = 1$. The control signals to other connectors are set to 0. The signals to other two-way switches are set to 00.

S4: $S_{12} = 10$. $S_{14} = 01$. $S_{16} = 10$. The control signals to other connectors are set to 0. The signals to other two-way switches are set to 00.

Answer :

- (a) $R3 = 0, R4 = 0$.
- (b) $R3 = 0, R4 = 1$.
- (c) $R3 = 1, R4 = 0$.
- (d) $R3 = 1, R4 = 1$.

Question 39

With reference to the simple processor as shown in the Appendix, Figure 2, it is assumed that the data in the memory locations $M1$ and $M2$ have already been copied to the registers RA and RB . What will be the logical operation once the following micro-instructions have been executed?

S1: $S_{12} = 01$ and $S_{15} = 10$. The control signals to other connectors are set to 0. The signals to all two-way switches are set to 00.

S2: $S_{12} = 10$ and $S_{13} = 01$. The control signals to other connectors are set to 0. The signals to all two-way switches are set to 00.

S3: $S_1 = S_8 = 1$. The control signals to other connectors are set to 0. The signals to all two-way switches are set to 00.

S4: $S_{12} = 10$, $S_{14} = 01$ and $S_{16} = 10$. The control signals to all connectors are set to 0. The signals to other two-way switches are set to 00.

S5: $S_{13} = 10$ and $S_{15} = 01$. The control signals to all connectors are set to 0. The signals to other two-way switches are set to 00.

S6: $S_2 = S_5 = S_9 = 1$. The control signals to other connectors are set to 0. The signals to other two-way switches are set to 00.

S7: $S_{12} = 10$, $S_{14} = 01$ and $S_{15} = 10$. The control signals to other connectors are set to 0. The signals to other two-way switches are set to 00.

What of the following instruction have been executed?

Answer :

(a) $R1 = (\neg RA)RB$ and $R2 = \neg RA$.

(b) $R1 = RA(\neg RB)$ and $R2 = \neg RA$.

(c) $R1 = (\neg RA)RB$ and $R2 = \neg RB$.

(d) $R1 = RA(\neg RB)$ and $R2 = \neg RB$.

(e) None of the above.

Question 40

With reference to the simple processor as shown in the Appendix, Figure 2, which of the following micro-program(s) can perform the logical operation.

$$Z = \neg A \oplus \neg B,$$

where $\neg A$ refers to logical NOT A. That is to say, once the data A (resp. B) has been copied to RA (resp. RB) and the micro-program has been executed, the result Z will appear in RZ .

(i) 7-Step micro-program.

S1: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S2: $S_{14} = 01$ and $S_{15} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S3: $S_{13} = 01$ and $S_{12} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S4: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S5: $S_{14} = 01$ and $S_{13} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S6: $S_{15} = 01$ and $S_{12} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S7: $S_4 = S_7 = S_{11} = 1$. Other connectors and switches are set to 'Disconnection' mode.

(ii) 8-Step micro-program.

S1: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S2: $S_{14} = 01$ and $S_{16} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S3: $S_{13} = 01$ and $S_{12} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S4: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S5: $S_{14} = 01$ and $S_{13} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S6: $S_{16} = 01$ and $S_{12} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S7: $S_4 = S_7 = S_{11} = 1$. Other connectors and switches are set to 'Disconnection' mode.

S8: $S_{14} = 01$ and $S_{15} = 10$. Other connectors and switches are set to 'Disconnection' mode.

(iii) Two-step micro-program.

S1: $S_4 = S_7 = S_{11} = 1$. Other connectors and switches are set to 'Disconnection' mode.

S2: $S_{14} = 01$ and $S_{15} = 10$. Other connectors and switches are set to 'Disconnection' mode.

Answer:

- (a) (i) and (ii).
- (b) (ii) and (iii).
- (c) (i) and (iii).
- (d) (i), (ii) and (iii).
- (e) None of the above.

Question 41

With reference to the simple processor as shown in the Appendix, Figure 2, which of the following micro-program(s) can perform the logical operation.

$$R1 = \neg A \oplus \neg B,$$

where $\neg A$ refers to logical NOT A. That is to say, once the data A (resp. B) has been copied to RA (resp. RB) and the micro-program has been executed, the result will appear in $R1$.

(i) 7-Step micro-program.

S1: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S2: $S_{14} = 01$ and $S_{15} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S3: $S_{13} = 01$ and $S_{12} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S4: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S5: $S_{14} = 01$ and $S_{13} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S6: $S_{15} = 01$ and $S_{12} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S7: $S_4 = S_7 = S_{11} = 1$. Other connectors and switches are set to 'Disconnection' mode.

(ii) 8-Step micro-program.

S1: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S2: $S_{14} = 01$ and $S_{16} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S3: $S_{13} = 01$ and $S_{12} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S4: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S5: $S_{14} = 01$ and $S_{13} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S6: $S_{16} = 01$ and $S_{12} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S7: $S_4 = S_7 = S_{11} = 1$. Other connectors and switches are set to 'Disconnection' mode.

S8: $S_{14} = 01$ and $S_{15} = 10$. Other connectors and switches are set to 'Disconnection' mode.

(iii) Two-step micro-program.

S1: $S_4 = S_7 = S_{11} = 1$. Other connectors and switches are set to 'Disconnection' mode.

S2: $S_{14} = 01$ and $S_{15} = 10$. Other connectors and switches are set to 'Disconnection' mode.

Answer:

- (a) (i) and (ii).
- (b) (ii) and (iii).
- (c) (i) and (iii).
- (d) (i), (ii) and (iii).
- (e) None of the above.

Question 42

With reference to the figure as shown in Figure 3, the initial conditions of the processor is set to be following.

$$S_1 = S_2 = S_3 = 0. \quad S_{12} = S_{13} = S_{14} = 00.$$

$$A1 = A2 = 0. \quad R/W = 00.$$

$$R1 = R2 = R3 = R4 = 0.$$

$$RA = 1. \quad RB = 0. \quad RZ = 0.$$

What will be the content of RZ and $R1$ if the following micro-program has been executed?

$$S1: S_1 = S_2 = S_3 = 1. \quad S_{12} = S_{13} = S_{14} = 00. \\ A1 = A2 = 0. \quad R/W = 00.$$

$$S2: S_1 = S_2 = S_3 = 0. \quad S_{12} = S_{13} = 10. \quad S_{14} = 01. \\ A1 = A2 = 0. \quad R/W = 00.$$

$$S3: S_1 = S_2 = S_3 = 1. \quad S_{12} = S_{13} = S_{14} = 00. \\ A1 = A2 = 0. \quad R/W = 00.$$

$$S4: S_1 = S_2 = S_3 = 0. \quad S_{12} = S_{13} = 00. \quad S_{14} = 01. \\ A1 = A2 = 0. \quad R/W = 10.$$

Answer :

(a) $RZ = 0, R1 = 0.$

(b) $RZ = 0, R1 = 1.$

(c) $RZ = 1, R1 = 0.$

(d) $RZ = 1, R1 = 1.$

Question 43

With reference to the figure as shown in Figure 3, the initial conditions of the processor is set to be following.

$$S_1 = S_2 = S_3 = 0. \quad S_{12} = S_{13} = S_{14} = 00.$$

$$A1 = A2 = 0. \quad R/W = 00.$$

$$R1 = R2 = R3 = R4 = 0.$$

$$RA = 0. \quad RB = 1. \quad RZ = 0.$$

What will be the content of $R1$ and $R2$ if the following micro-program has been executed?

$$S1: S_1 = S_2 = S_3 = 0. \quad S_{12} = 00. \quad S_{13} = 01. \quad S_{14} = 00. \\ A1 = 0. \quad A2 = 0. \quad R/W = 10.$$

$$S2: S_1 = S_2 = S_3 = 0. \quad S_{12} = 01. \quad S_{13} = 10. \quad S_{14} = 00. \\ A1 = 0. \quad A2 = 0. \quad R/W = 00.$$

$$S3: S_1 = S_2 = S_3 = 1. \quad S_{12} = 00. \quad S_{13} = 00. \quad S_{14} = 00. \\ A1 = 0. \quad A2 = 0. \quad R/W = 00.$$

$$S4: S_1 = S_2 = S_3 = 0. \quad S_{12} = 00. \quad S_{13} = 00. \quad S_{14} = 01. \\ A1 = 0. \quad A2 = 1. \quad R/W = 10.$$

$$S5: S_1 = S_2 = S_3 = 0. \quad S_{12} = 10. \quad S_{13} = 10. \quad S_{14} = 00. \\ A1 = 0. \quad A2 = 0. \quad R/W = 01.$$

$$S6: S_1 = S_2 = S_3 = 1. \quad S_{12} = 00. \quad S_{13} = 00. \quad S_{14} = 00. \\ A1 = 0. \quad A2 = 0. \quad R/W = 00.$$

$$S7: S_1 = S_2 = S_3 = 0. \quad S_{12} = 00. \quad S_{13} = 10. \quad S_{14} = 01. \\ A1 = 0. \quad A2 = 0. \quad R/W = 00.$$

$$S8: S_1 = S_2 = S_3 = 0. \quad S_{12} = 10. \quad S_{13} = 00. \quad S_{14} = 00. \\ A1 = 0. \quad A2 = 1. \quad R/W = 01.$$

$$S9: S_1 = S_2 = S_3 = 1. \quad S_{12} = 00. \quad S_{13} = 00. \quad S_{14} = 00. \\ A1 = 0. \quad A2 = 0. \quad R/W = 00.$$

$$S10: S_1 = S_2 = S_3 = 0. \quad S_{12} = 00. \quad S_{13} = 00. \quad S_{14} = 01. \\ A1 = 1. \quad A2 = 0. \quad R/W = 10.$$

Answer :

(a) $R1 = 0, R2 = 0.$

(b) $R1 = 0, R2 = 1.$

(c) $R1 = 1, R2 = 0.$

(d) $R1 = 1, R2 = 1.$

Question 44

Here are four memory locations, $M1$, $M2$, $M3$ and $M4$. Refer to the artificial CPU and its commands, what will be the content of $M4$ if the following commands are executed?

```
DEF M1 3
DEF M2 5
DEF M3 2
```

```
MOV IA M1
MOV IB M2
ADD IA IB
MOV IA OUT
MOV IB M3
MUL IA IB
MOV M4 OUT
```

Answer :

(a) 16.

(b) 21.

(c) 25.

(d) 30.

(e) None of the above.

Question 45

Here are four memory locations, $M1$, $M2$, $M3$ and $M4$. Refer to the artificial CPU and its commands, what will be the content of $M4$ if the following commands are executed?

```
DEF M1 3
DEF M2 5
DEF M3 2

MOV IA M1
MOV IB M2
ADD IA IB
ADD IA IB
MOV IA OUT
MOV IB M3
MUL IA IB
MOV M4 OUT
```

Answer :

- (a) 16.
- (b) 21.
- (c) 26.
- (d) 32.
- (e) None of the above.

Question 46

Here are four memory locations, $M1$, $M2$, $M3$ and $M4$. Refer to the artificial CPU and its commands, what will be the contents of the registers IB and OUT if the following commands are executed?

```
DEF M1 3
DEF M2 5
DEF M3 2

MOV IA M1
MOV IB M2
ADD IA IB
MOV IA OUT
MOV IB M3
ADD IA IB
MOV M4 OUT
```

Answer :

- (a) $IB = 0$ and $OUT = 0$.
- (b) $IB = 2$ and $OUT = 0$.
- (c) $IB = 0$ and $OUT = 10$.
- (d) $IB = 2$ and $OUT = 10$.
- (e) None of the above.

Question 47

What will be the content of $M4$ if the following program segment is executed?

```
DEF M1 16
DEF M2 22
DEF M3 10

MOV IA M1
MOV IB M2
CMP IA IB
MOV M4 OUT
MOV IA M2
MOV IB M3
CMP IA IB
MOV IA OUT
MOV IB M4
ADD IA IB
MOV M4 OUT
```

Answer :

- (a) 28.
- (b) 30.
- (c) 32.
- (d) 34.
- (e) None of the above.

Question 48

Find the value of $M3$ after the following program segment has been executed.

```
-----
DEF M1 13
DEF M2 12

MOV IA M1
SHL IA 00000010
MOV IA OUT
MOV IB M2
ADD IA IB
MOV M3 OUT
-----
```

Answer :

- (a) $M3 = 25$.
- (b) $M3 = 38$.
- (c) $M3 = 51$.
- (d) $M3 = 64$.
- (e) None of the above.

Question 49

Find the value of $M3$ after the following program segment has been executed.

```

-----
DEF M1 13
DEF M2 12

MOV IA M1
SHL IA 0000010
MOV IA OUT
MOV IB M2
ADD IA IB
MOV M3 OUT
-----

```

Which of the following mathematical equation is identical to the operation of the following program segment?

Answer :

- (a) $M3 = 2 \times M1 + M2$.
- (b) $M3 = 2 \times (M1 + M2)$.
- (c) $M3 = 4 \times M1 + M2$.
- (d) $M3 = 4 \times (M1 + M2)$.
- (e) None of the above.

Question 50

Given that there are five memories $M1, M2, M3, M4$ and $M5$. Here is the program segment to instruct the circuit.

```

-----
MOV IA M1
MOV IB M2
MUL IA IB
MOV IA OUT
MOV IB M3
MUL IA IB
MOV IA OUT
MOV IB M4
SUB IA IB
MOV M5 OUT
-----

```

Which of the following mathematical equation is identical to the operation of the following program segment?

Answer :

- (a) $M5 = M4 - M1 \times M2 \times M3$.
- (b) $M5 = M4 - (M1 + M2) \times M3$
- (c) $M5 = M1 \times M2 \times M3 - M4$.
- (d) $M5 = (M1 + M2) \times M3 - M4$.
- (e) None of the above.

APPENDIX

In this appendix, it includes the information about a simple processor, an artificial CPU and the source codes of five programs. Please read them carefully!

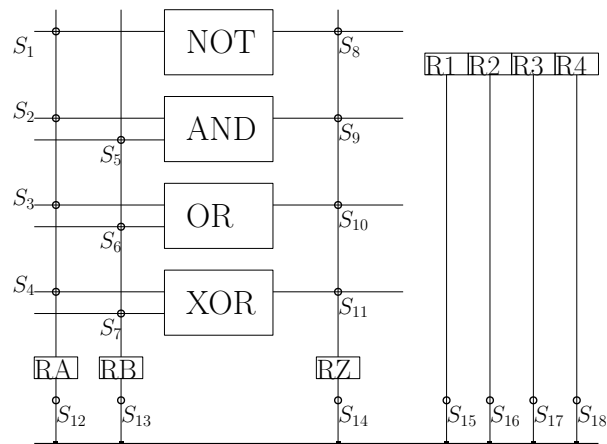
A. Processor with 4 Logic Gates

A simple processor, with a sector of four logic gates and a sector of four registers, shown in Figure 2. Each register is associated with a two-way switch. The signals to be fed to the switch and the corresponding actions are depicted in the following table.

S_i	Action
00	Disconnect.
01	Read from register.
10	Write to register.

For each connector, its control signal is either '0' (for disconnection) and '1' (for connection).

$$\text{Connection} = \begin{cases} \text{Connect} & \text{if } S_i = 1, \\ \text{Disconnect} & \text{if } S_i = 0. \end{cases}$$



Two-Way Switches: Disconnected (00); Down (01), Up (10).

($S_{12}, S_{13}, S_{14}, S_{15}, S_{16}, S_{17}, S_{18}$)

Connectors: Disconnected (0), Connected (1).

($S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8, S_9, S_{10}, S_{11}$)

Figure 2: A processor with four logic gates. Switches S_1 to S_{11} are simple switches (i.e. connectors). S_{12} to S_{18} are two-way switches.

B. Processor with a NAND Gate

Figure 3 shows a simple processor with single NAND gate inside. Switches S_1, S_2 and S_3 are simple

switches (i.e. connectors). S_{12} , S_{13} and S_{14} are two-way switches. The signals sending to $A1$, $A2$ and R/W together with the corresponding actions are depicted in the following table.

A1	A2	R/W	Action
0	0	01	Read data from $R1$
0	1	01	Read data from $R2$
1	0	01	Read data from $R3$
1	1	01	Read data from $R4$
0	0	10	Write data to $R1$
0	1	10	Write data to $R2$
1	0	10	Write data to $R3$
1	1	10	Write data to $R4$
x	x	00	Disconnection

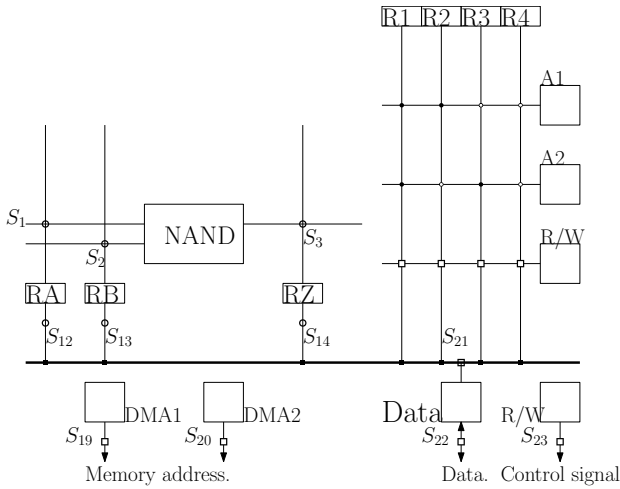
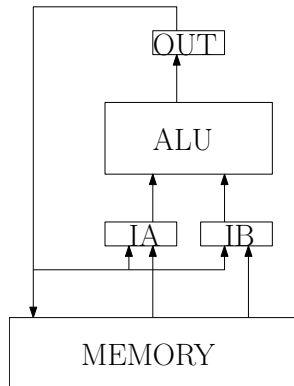


Figure 3: A processor with single NAND gate.

C. Artificial CPU

Below is a simple circuit. It consists of a **memory** with 16 memory spaces (from $M1$ to $M16$), an **ALU block**, 2 **input registers** (IA and IB) and one **output register** (OUT). $M1$ to $M16$, IA , IB and OUT are all 8 bits long. Numbers are represented in 2 's *compliment* format.



Eleven commands (MOV, ADD, SUB, MUL, DIV, CMP, SHL, SHR, DEF, MSK and IF) are provided for instructing the above circuit. The syntax and the descriptions of these commands are depicted in Table 1.

Table 1: Commands for using the CPU.

Syntax	Description
MOV X Y	Copy the content of Y to X
ADD X Y	$OUT = X + Y$.
SUB X Y	$OUT = X - Y$.
MUL X Y	$OUT = X \times Y$.
DIV X Y	$OUT = X/Y$.
CMP X Y	$OUT = b_1b_2b_3b_4b_5b_6b_7b_8$. $b_i = 0$ if $X_i = Y_i$. $b_i = 1$ if $X_i \neq Y_i$.
SHL X Y	OUT is the content of X shifting left Y bits.
SHR X Y	OUT is the content of X shifting right Y bits.
DEF X N	Define X as the number N.
MSK X M	Mask the value of X by M.
IF ELSE	Condition statement.

D. Notes on CPU Commands

- For the "CMP" command, if $X = 0110$ and $Y = 1101$, $OUT = 1011$.
- For "SHL" and "SHR" commands, the content of Y can only be one of the following.

Y	Meaning
10000000	(Shift 7 bits)
01000000	(Shift 6 bits)
00100000	(Shift 5 bits)
00010000	(Shift 4 bits)
00001000	(Shift 3 bits)
00000100	(Shift 2 bits)
00000010	(Shift 1 bits)
00000001	(No shift)

For example, if

$$X = 00011000, Y = 00000100,$$

the OUT of "SHL X Y" is 01100000 and the OUT of "SHR X Y" is 00000110.

- For the "DEF" command, N must be a number in *decimal* form. X can only be a memory location. "DEF" command is not applicable for assigning values to a register. It is used to assign a value to a memory location. For example, "DEF M1 12" means that memory location

$M1$ will be assigned with a value 12. Therefore, $M1 = 00001100$.

- For the "MSK" command, it is used for masking a register (either IA or IB) by the mask M (in binary). The mask must be 8 bits long.

Suppose that the content of IA and M are defined as follows :

$$IA = 01001001, M = 11110000.$$

Then, the output OUT will be "01000000". The last four bits are masked. Here is an example.

```

-----
DEF M1 45
MOV IA M1
MSK IA 00001111
MOV M2 OUT
-----

```

Initially, $M1$ is assigned with value 45. In binary form, the content reads "00101101". Thus, the output OUT is "00001101".

- The "IF-ELSE" command is an advanced level command. It is for conditional statement. Once it is executed, the CPU will perform multiple steps in order to make it work. You do not need to know the detail how it works. In terms of its usage, it is simple. Here is an example.

```

-----
DEF M1 1
DEF M2 2
DEF M3 1

MOV IA M1
IF IA == 0
    MOV IA M2
    MOV IB M3
    ADD IA IB
    MOV M4 OUT
ELSE
    MOV IA M1
    ADD IB M2
    MOV M4 OUT
ENDIF
-----

```

Command "IF" checks if the content of IA is identical to "0". If it is, it will perform $M2 + M3$ and output the result to $M4$. Otherwise, it will perform $M1 + M2$ and output the result to $M4$.

```

-----
DEF M1 1
DEF M2 2

```

```

DEF M3 1

MOV IA M1
IF IA == 0
    MOV IA M2
    MOV IB M3
    ADD IA IB
    MOV M4 OUT
ENDIF
-----

```

In this example, the CPU performs $M2 + M3$ only if IA is zero. Otherwise, it performs nothing.

- For the "IF-ELSE" command, the following conditions are allowed for you to define. Here NUM must be stated in decimal form but not in binary.

```

-----
IA == NUM
IA > NUM
IA >= NUM
IA < NUM
IA <= NUM
-----

```