CS2021 ASSIGNMENT 6 (Due Date: Oct 22, 2021)

Instructions: This assignment consists of two sections. Section A consists of four questions. Section B consists of three questions. You have to answer all of them.

Binary Numbers

Question 1

Suppose a number represented in the following 16-bit sign-magnitude fix-point format.

```
sxxxxxxxxxxx.xxxx
```

For this representation format, zero is the smallest nonnegative number that can be represented. It binary code is given below.

```
0000000000000000
```

(a) What is the second smallest nonnegative number (in decimal form) that can be represented?

(b) What is the binary code for the second smallest nonnegative number that can be represented?

(c) What is the precision error of this fix-point format?

(d) What is the total number of decimal numbers that can be represented by this format?

Precision error of a number representation format is defined as the absolute value between two consecutive numbers that can be represented by the format.

Question 2

Suppose a binary number is represented by the following 8-bit sign-magnitude fix-point format.

```
sxxxx.xxx
```

What are the values of the following binary numbers?

(a) 00011100.

(b) 10011100.

(c) 10011001.

(d) 00111101.

Question 3

It is clear that the binary numbers in Question 2(b) and Question 2(c) are negative numbers. What are the binary codes for these numbers if they are represented in 8-bit 2's complement format?

Question 4

Given that X and Y are two numbers represented in following format.

```
sxxxx.xxx
```

Their actual bit patterns are given below.

```
X = 00011100
Y = 10010010
```

What is the value $X \times Y$ in the above 8-bit sign-magnitude format?

Processor and Computer

The following questions are about the concepts presented in the lecture note '*Processor and Computer*'.

Question 5

(a) Apart from the clock speed, state other factor(s) that could determine the completion time of an instruction.

(b) State the reason(s) why the set of instruction provided by one processor could be different from the set of instruction provided by another processor.

(c) In a processor, a special unit is responsible for the generation of the sequence of micro-instructions for an instruction. This process is called instruction decode. State the name of the unit which is responsible for instruction decode.

(d) What is(are) the usage(s) of the registers in a processor?

Question 6

With reference to the four-logic-gate processor as shown in Figure 1, design the micro-instructions for the following logical operations. It is assumed that the value of A (resp. B) has already been stored in the register RA (resp. RB). The outcome Z is going to be stored in the register RZ.

(a) $R1 = \neg A$.

(b) $Z = \neg A \oplus \neg B$.

(c) $Z = A + (\neg A \oplus \neg B)$.

Here, $\oplus$ is the XOR operator and $\neg A = \bar{A}$.

Question 7

With reference to the four-logic-gate processor as shown in Figure 5, design the micro-instructions for the following logical operations. It is assumed that the value of A (resp. B) has already been stored in the register RA (resp. RB). The outcome Z is going to be stored in the register RZ.

(a) $R1 = \neg A$.

(b) $Z = \neg A \oplus \neg B$.

(c) $Z = A + (\neg A \oplus \neg B)$.

Here, $\oplus$ is the XOR operator and $\neg A = \bar{A}$.