CS2021 ASSIGNMENT 6 Answer

Instructions: This assignment consists of two sections. Section A consists of four questions. Section B consists of three questions. You have to answer all of them.

Binary Numbers

Question 1

Suppose a number represented in the following 16-bit sign-magnitude fix-point format.

`sxxxxxxxxxxx.xxxx`

For this representation format, zero is the smallest nonnegative number that can be represented. Its binary code is given below.

`0000000000000000`

(a) What is the second smallest nonnegative number (in decimal form) that can be represented?

Answer:

$$\begin{aligned} 0000000000000001 &= 000000000000.0001 \\ &= 2^{-4}. \end{aligned}$$

(b) What is the binary code for the second smallest nonnegative number that can be represented?

Answer: 0000000000000001.

(c) What is the precision error of this fix-point format?

Answer: The precision error is 2^{-4}.

(d) What is the total number of decimal numbers that can be represented by this format?

Answer: For nonnegative numbers, 2^{15} decimal numbers can be represented, from 0 to $2^{15} - 1$ (i.e. 0000000000000000 to 0111111111111111).

For negative numbers, $2^{15} - 1$ decimal numbers can be represented, from -1 to $-(2^{15} - 1)$ (i.e. 0000000000000000 to 1111111111111111). Note that 1000000000000000 is not a number.

Therefore, the total number of decimal numbers that can be represented by this format is $2^{16} - 1$.

Precision error of a number representation format is defined as the absolute value between two consecutive numbers that can be represented by the format.

Question 2

Suppose a binary number is represented by the following 8-bit sign-magnitude fix-point format.

`sxxxx.xxx`

What are the values of the following binary numbers?

(a) 00011100.

Answer: 3.5.

(b) 10011100.

Answer: -3.5.

(c) 10011001.

Answer: -3.125.

(d) 00111101.

Answer: 7.625.

Question 3

It is clear that the binary numbers in Question 2(b) and Question 2(c) are negative numbers. What are the binary codes for these numbers if they are represented in 8-bit 2's complement format?

Answer: (b) 111001100. (c) 11100111.

Question 4

Given that X and Y are two numbers represented in following format.

`sxxxx.xxx`

Their actual bit patterns are given below.

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X = 00011100
Y = 10010010
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What is the value $X \times Y$ in the above 8-bit sign-magnitude format?

Answer: Let Y_L and Y_R be the integer and fractional part of the magnitude of Y.

$$Y_L = 00010.000, \quad Y_R = 00000.010.$$

Then, we can write $X \times Y$ as $X \times Y_L + X \times Y_R$.

$$\begin{aligned} X \times Y_L &= 00011.100 \times 00010.000 \\ &= 00111.000. \quad \text{(Shift Left)} \\ X \times Y_R &= 00011.100 \times 00000.010 \\ &= 00000.111. \quad \text{(Shift Right)} \end{aligned}$$

As X is positive and Y is negative, $X \times Y$ is negative and

$$X \times Y = 10111111.$$

Processor and Computer

The following questions are about the concepts presented in the lecture note '*Processor and Computer*'.

Question 5

(a) Apart from the clock speed, state other factor(s) that could determine the completion time of an instruction.

Answer: The architecture of the processor and the design of the micro-instructions for an instruction.

(b) State the reason(s) why the set of instruction provided by one processor could be different from the set of instruction provided by another processor.

Answer: It is because different processors have different architectures. The set of micro-instructions could thus be different from one processor to another. In the end, the set of instruction provided by one processor could be different from the set of instruction provided by another processor.

(c) In a processor, a special unit is responsible for the generation of the sequence of micro-instructions for an instruction. This process is called instruction decode. State the name of the unit which is responsible for instruction decode.

Answer: Control unit.

(d) What is(are) the usage(s) of the registers in a processor?

Answer: (i) The registers act as a temporarily working space for storing the data (copied from the main memory) for the completion of an instruction. (ii) The registers act as a temporarily working space for storing the data generated during the execution of a micro-instruction, for later use.

Question 6

With reference to the four-logic-gate processor as shown in Figure 1, design the micro-instructions for the following logical operations. It is assumed that the value of A (resp. B) has already been stored in the register RA (resp. RB). The outcome Z is going to be stored in the register RZ.

In (a), (b) and (c), $\oplus$ is the XOR operator and $\neg A = \bar{A}$.

(a) $R1 = \neg A$.

Answer:

S1: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S2: $S_{14} = 01$ and $S_{15} = 10$. Other connectors and switches are set to 'Disconnection' mode.

(b) $Z = \neg A \oplus \neg B$.

Answer (1): This instruction could be accomplished by the following 7-step micro-program.

S1: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S2: $S_{14} = 01$ and $S_{15} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S3: $S_{13} = 01$ and $S_{12} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S4: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S5: $S_{14} = 01$ and $S_{13} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S6: $S_{15} = 01$ and $S_{12} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S7: $S_4 = S_7 = S_{11} = 1$. Other connectors and switches are set to 'Disconnection' mode.

Answer (2): The truth table of $\neg A \oplus \neg B$ is depicted in the following.

A	B	$\neg A$	$\neg B$	$\neg A \oplus \neg B$
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	0

Hence, $\neg A \oplus \neg B = A \oplus B$. The instruction could be accomplished by the following one-step micro-program.

S1: $S_4 = S_7 = S_{11} = 1$. Other connectors and switches are set to 'Disconnection' mode.

(c) $Z = A + (\neg A \oplus \neg B)$.

Answer: From the previous question, it is know that

$$\neg A \oplus \neg B = A \oplus B.$$

The truth table of $A + \neg A \oplus \neg B$ is depicted in the following.

A	B	$A \oplus B$	$A + A \oplus B$
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	1

Clearly, $A + (A \oplus B) = A + B$. The instruction could be accomplished by the following one-step micro-program.

S1: $S_3 = S_6 = S_{10} = 1$. Other connectors and switches are set to 'Disconnection' mode.

Question 7

With reference to the four-logic-gate processor as shown in Figure 5, design the micro-instructions for the following logical operations. It is assumed that the value of A (resp. B) has already been stored in the register RA (resp. RB). The outcome Z is going to be stored in the register RZ.

(a) $R1 = \neg A$.

Answer:

S1: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode. $R/W = 00$.

S2: $S_{14} = 01$, $A_1 = 0$, $A_2 = 0$ and $R/W = 10$. Other connectors and switches are set to 'Disconnection' mode.

(b) $Z = \neg A \oplus \neg B$.

Answer (1): This instruction could be accomplished by the following 7-step micro-program.

S1: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode. $R/W = 00$.

S2: $S_{14} = 01$, $A_1 = 0$, $A_2 = 0$ and $R/W = 10$. Other connectors and switches are set to 'Disconnection' mode.

S3: $S_{13} = 01$, $S_{12} = 10$ and $R/W = 00$. Other connectors and switches are set to 'Disconnection' mode.

S4: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode. $R/W = 00$.

S5: $S_{14} = 01$ and $S_{13} = 10$. Other connectors and switches are set to 'Disconnection' mode. $R/W = 00$.

S6: $S_{12} = 10$ $A_1 = 0$, $A_2 = 0$ and $R/W = 01$. Other connectors and switches are set to 'Disconnection' mode.

S7: $S_4 = S_7 = S_{11} = 1$. Other connectors and switches are set to 'Disconnection' mode. $R/W = 00$.

Answer (2): The instruction could be accomplished by the following one-step micro-program.

S1: $S_4 = S_7 = S_{11} = 1$. Other connectors and switches are set to 'Disconnection' mode.

(c) $Z = A + (\neg A \oplus \neg B)$.

Answer: The instruction could be accomplished by the following one-step micro-program.

S1: $S_3 = S_6 = S_{10} = 1$. Other connectors and switches are set to 'Disconnection' mode.

Here, $\oplus$ is the XOR operator and $\neg A = \bar{A}$.