CS2022 ASSIGNMENT 6 (Due Date: Oct 21, 2022)

Instructions: In this assignment, there are eight questions. The last three questions are multiple-choice questions. You have to answer all of them.

Question 1

Figure 1 shows a digital circuit with four full adders. For the left input of each full adder, it is always input with '0'. For the full adder associated with Z_0, the right input is always '1'. The input $A = A_3A_2A_1A_0$ is restricted to $0XXX$, where X is either 0 or 1.

(a) What will be the output $Z = Z_4Z_3Z_2Z_1Z_0$ if $A = 0011$?

(b) What will be the output $Z = Z_4Z_3Z_2Z_1Z_0$ if $A = 0111$?

(c) What is the digital circuit used for?

Answer:

(a) $Z = 1101$.

(b) $Z = 1001$.

(c) It is a 2's complement converter. Once a positive integer A is fed in, the circuit outputs the 2's complement of $-A$.

Question 2

(a) In a processor, there must have a module called *control unit* or *instruction decode unit*. What is it used for?

(b) What is the difference between *instruction* and *microinstruction*?

(c) What is a microprogram?

(d) What factor determines the design of a microprogram?

(e) State three factors which determine the performance of a processor.

Answer:

(a) Once an instruction (in a form of machine code) has fed in a CPU, the control unit generates a sequence of microinstructions controlling the switches in the CPU.

(b) An instruction is higher level than a microinstruction. Each instruction is an instruction for the CPU. Each microinstruction is an instruction for controlling the switches in a CPU.

(c) A microprogram is a sequence of microinstructions to accomplish the job to be done for an instruction.

(d) The architecture of a CPU.

(e) The architecture of a processor, the microprogram design and the clock speed (i.e. the number of cycles a CPU executes per second).

Question 3

(a) Each modern computer must have five necessary hardware components. What are they?

(b) State the reasons why RAM is needed in a computer system?

(c) State at least two differences between a CISC processor and a RISC processor.

(d) State two CISC processors which can be found in a computer or a cell phone.

(e) State two RISC processors which can be found in a computer or a cell phone.

Answer:

(a) A processor, a memory device, an input device, an output device and a network communication device.

(b) One reason is because the access time between a processor and a RAM is much smaller than the access time between a processor and the main memory (i.e. the harddisk or solid state drive).

With RAM, together with other memory access devices like a chip called direct memory access (DMA), block of data to be processed by the program could be *prefetched* from the main memory (i.e. the HD or SSD) and put into the RAM. While the CPU is processing the data, it can then get the data from the RAM instead of the main memory. The completion time of the program can be largely reduced.

During system initialization, the CPU needs to get the instructions of the operating system from

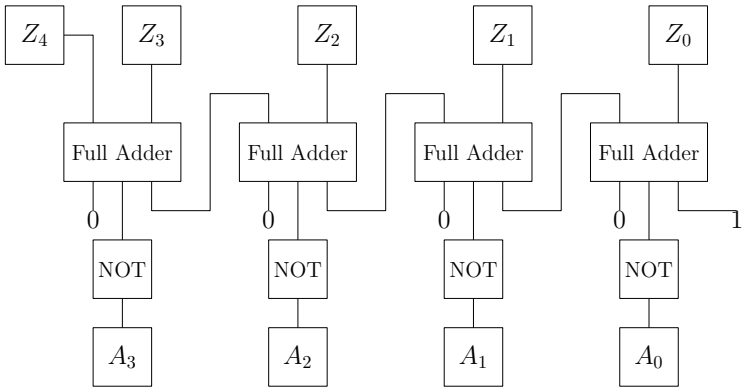

Figure 1: Digital circuit for Question 1.

the main memory. With RAM, block of instructions can then be prefetched from the main memory to the RAM. Once the execution of an instruction has completed, the CPU can then get the next instruction directly from the RAM. In this regard, the time spent in system initialization can be largely reduced.

(c) (i) The number of instructions in the set instructions for a CISC processor is larger than the number of instructions for a RISC processor. (ii) The architecture of a CISC processor is usually much more complicated than a RISC processor.

(d) Intel Core i7 and AMD Zen.

(e) Apple A series processor for iPhone, Apple M series processor for Mac computers and the graphical processing units (GPUs) form Nvidia.

Question 4

With reference to the 4-logic-gate processor architecture as shown in Figure 5 in the lecture note *Processor and Computer*, design the micro-instructions for the following logical operations. It is assumed that the value of A (resp. B) has already been stored in the register RA (resp. RB).

(a) $R1 = \neg A$.

(b) $R2 = \neg B$.

(c) $Z = (\neg A) \oplus (\neg B)$.

(d) $Z = A + ((\neg A) \oplus (\neg B))$.

Here $\neg$ refers to NOT operation, $\oplus$ refers to XOR operation and $+$ refers to OR operation. You answers have to be conformed to the format as shown in Figure 4 in the lecture note *Processor and Computer*.

Answer:

(a) (i) $S_1 = S_8 = 1$, other switches are in disconnection mode. (ii) $S_{14} = 01$, $A_1 = 0$, $A_2 = 0$, $R/W = 10$ and other switches are in disconnection mode.

(b) (i) $S_{12} = 10$, $S_{13} = 01$ and other switches are in disconnection mode. (ii) $S_1 = S_8 = 1$, other switches are in disconnection mode. (iii) $S_{14} = 01$, $A_1 = 0$, $A_2 = 1$, $R/W = 10$ and other switches are in disconnection mode.

(c) (i) $S_4 = S_7 = S_{11} = 1$ and other switches are in disconnection mode.

(d) (i) $S_3 = S_6 = S_{10} = 1$ and other switches are in disconnection mode.

Question 4

With reference to the 4-logic-gate processor architecture as shown in Figure 5 in the lecture note *Processor and Computer*, design the micro-instructions for the following logical operations. It is assumed that the initial setting for RA and RB are 1 and 0. The contents of the other registers are set to '0'.

S1. $R1 = \neg A$.

S2. $R2 = \neg B$.

S3. $R3 = (\neg A) \oplus (\neg B)$.

Here $\neg$ refers to NOT operation and $\oplus$ refers to XOR operation.

What will be the contents of RA, RB, RZ, $R1$, $R2$, $R3$ and $R4$ after the above steps have been executed ?

Answer: $RA = RB = RZ = 0$, $R_1 = 0$, $R_2 = 1$, $R_3 = R_4 = 0$.

Question 5

With reference to the single-NAND-gate processor as shown in Figure 1 in *Processor and Computer (Supplementary)*, design the micro-instructions for the realization of the following instructions.

(a) NOT RA.

(b) AND RA RB.

You answers have to be conformed to the format as shown in Figure 4 in the lecture note *Processor and Computer*. That is to say, you need to depict the control signals to be sent to the switches, the address bits A_1 and A_2; and the signal for R/W.

Answer:

(a) (i) $S_{12} = 01$, $S_{13} = 10$, $A_1 = A_2 = 0$ and $R/W = 00$. (ii) $S_1 = S_2 = S_3 = 1$, $A_1 = A_2 = 0$ and $R/W = 00$.

(b) (i) $S_1 = S_2 = S_3 = 1$, $A_1 = A_2 = 0$ and $R/W = 00$. (ii) $S_{12} = S_{13} = 10$, $S_{14} = 01$, $A_1 = A_2 = 0$ and $R/W = 00$.(iii) $S_1 = S_2 = S_3 = 1$, $A_1 = A_2 = 0$ and $R/W = 00$.

Question 6

Refer to the artificial CPU and its commands, what will be the content of $M4$ if the following commands are executed?

```
DEF M1 1
DEF M2 2
DEF M3 5

MOV IA M1
IF IA == 0
   MOV IA M2
   MOV IA M2
   MOV IB M3
   ADD IA IB
   MOV M4 OUT
ELSE
   MOV IA M1
   MOV IA M1
   MOV IB M3
   MUL IA IB
   MOV M4 OUT
ENDIF
```

Answer: C.

(a) 2.

(b) 7.

(c) 5.

(d) 0.

(e) None of the above.

Question 7

What will be the content of $M4$ if the following program segment is executed?

```
DEF M1 16
DEF M2 22
DEF M3 10
MOV IA M1
MOV IB M2
CMP IA IB
CMP IA IB
MOV M4 OUT
MOV IA M2
MOV IB M3
CMP IA IB
CMP IA IB
MOV IA OUT
MOV IB M4
ADD IA IB
MOV M4 OUT
```

Answer: D.

(a) 28.

(b) 30.

(c) 32.

(d) 34.

(e) None of the above.

Question 8

Given that there are five memories M1, M2, M3, M4 and M5. Here is the program segment to instruct the circuit.

```
----------------
MOV IA M1
MOV IB M2
MUL IA IB
MOV IA OUT
MOV IB M3
MUL IA IB
MOV IA OUT
MOV IB M4
SUB IA IB
MOV M5 OUT
----------------
```

which of the following mathematical equation is identical to the operation of the following program segment?

Answer: C.

(a) $M5 = M4 - M1 \times M2 \times M3$.

(b) $M5 = M4 - (M1 + M2) \times M3$

(c) $M5 = M1 \times M2 \times M3 - M4$.

(d) $M5 = (M1 + M2) \times M3 - M4$.

(e) None of the above.