CS2022 ASSIGNMENT 7 (Due Date: Oct 28, 2022)

Instructions: You have to answer all of them.

Question 1

(a) In a computer, which hardware device is the key device to execute an instruction (in forms of machine code) of an operating system?

(b) In a computer, which hardware device is the key device to execute an instruction (in forms of machine code) of an application software, like Chrome?

(c) Once a computer has just been power on, a CPU will execute a dedicated instruction. This instruction is hardwired in a special read-only-memory (ROM) device. What is the name of this memory device?

(d) If two CPUs have different architectures, would it be possible that their sets of instructions be the same? [Hint: Consider Table 1 in the lecture note "Processor and Computer". If we would like to add the instruction "MOV RB RM" in the set of instructions for the processor shown in Figure 5, how could we make it possible?]

(e) In the lecture, I have introduced four levels of programming, namely high level, middle level, low level assembly language programming and the lowest level microprogramming. For the high level and middle level programming, state for each level one programming language which is developed for that level.

(f) In a computer, which device contains the instructions of the executable file of Chrome?

(g) In a computer, which device contains the instructions of the executable file of an operating system?

(h) Nowadays, almost all computers and cell phones must have a memory device called RAM. Why does the CPU not simply access directly to the hard disk or solid state drive which is the main memory?

(i) Direct memory access (DMA) is a hardware device specialized designed for the transferring between the RAM and the main memory. Describe how does it work.

(j) If a factory is an analogy to a processor, which role is the best analogy of a switch?

(k) If a factory is an analogy to a processor, which role is the best analogy of a microprogram designer?

(l) If a factory is an analogy to a processor, what is the best analogy of a memory device?

(m) If a factory is an analogy to a processor, what is the best analogy of an instruction?

(n) In between a processor and the main memory, there are four types of signals to be transferred. They are the "instruction", "data", "memory address" and "control signals". Let say, the number of bits for an instruction, a data or memory address is 16. In such case, the number of physical pins of a CPU will be larger than 48. To reduce the number of pins to be minimum, there are 16 pins for handling the signals "instruction", "data" and "memory address". Describe how does it work.

(o) With reference to the Section 3.4 "Process and Computer (Supplement)", which factors are used for program complexity? Note that a program could be a microprogram or a C program.

(p) State the names of two families (equivalently series) of operating systems.

(q) In a computer or a cell phone, there are so many hardware devices. To synchronize all these devices, there must be a special circuit or device to be connected to all these devices. What is the name of this circuit or device?

Answer:

(a) CPU.

(b) CPU.

(c) BIOS.

(d) Yes, it is possible. Two different CPUs with different architectures could have different microprograms to support the same instruction. Depending on the processor architecture, one microprogram might have more microinstructions than the other.

(e) Structural Query Language (SQL) is a high level programming language. C Language is a middle level programming language.

(f) The harddisk (equivalently harddrive) or the solid state drive (SSD).

(g) The harddisk (equivalently harddrive) or the solid state drive (SSD).

(h) The access time between the CPU and the harddisk (resp. solid state drive) is long. Some programs might need to process a large amount of data which is stored in the main memory. Without RAM, the completion time of any one of these programs will be too long.

With RAM, together with other memory access devices like a chip called direct memory access (DMA), block of data to be processed by the program could be *prefetched* from the main memory (i.e. the HD or SSD) and put into the RAM. While the CPU is processing the data, it can then get the data from the RAM instead of the main memory. The completion time of the program can be largely reduced.

During system initialization, the CPU needs to get the instructions of the operating system from the main memory. With RAM, block of instructions can then be prefetched from the main memory to the RAM. Once the execution of an instruction has completed, the CPU can then get the next instruction directly from the RAM. In this regard, the time spent in system initialization can be largely reduced.

(i) See the answer for (h).

(j) A human worker.

(k) An operational level manager, foreman, supervisor or team leader.

(l) A warehouse.

(m) A request for a service or production.

(n) First of all, it is noted that the time when a processor reads (resp. writes) data from (resp. to) the memory and the time when a processor reads an instruction must be different. Therefore, the pins for reading/writing data and reading instruction can be multiplexed into one set of 16 pins.

Second, to read/write a data (resp. read an instruction), the processor should have pins for the signal of memory address. To reduce the number of pins, reading/writing data from/to the memory device could be conducted in two steps (i.e. two clock cycles) instead of one step (i.e. one clock cycle).

S1. The processor sends memory address signal together with the control signal (R/W) to the memory device. The memory device *latches* this address signal in a set of registers. Let me call it memory address register (MAR). In this time around, the set of pins is responsible for memory address.

S2. In the second step, if the control signal is write, the processor outputs the data to the set of pins. The memory device simultaneously latches the signal from the set of pins to the memory location specified in the MAR. If the control signal is read, the content in the corresponding memory address is output to the set of pins. Simultaneously, the processor latches from the set of pins for the data.

Reading instruction from the memory device is conducted by the same two-step operation.

In this regard, the set of pins for memory address signal, the set of pins for data and the set of pins for instruction can be multiplexed as one set of pins, instead of three sets of pins. In essence, an instruction is just a sequence of binary number. It could be considered as a type of data. So, this set of pins is named 'AD' standing for "Address and Data".

(o) In accordance with the lecture note, program complexity is simply defined as the number of steps needed for a processor to complete the task to be accomplished by a program.

(p) Windows series, MacOS series and Unix series.

(q) Clock circuit.

Question 2

Three numbers have been stored in M1, M2 and M3. Which of the following program segments can correctly give the output of the following formulae?

$$M4 = M1 + M2 \times M3.$$

Answer: C.

(a)
```
----------------
MOV IA M1
MOV IB M2
MUL IA IB
MOV IA OUT
MOV IB M3
ADD IA IB
MOV M4 OUT
----------------
```

(b)
```
----------------
MOV IA M1
MOV IB M2
ADD IA IB
MOV IA OUT
MOV IB M3
MUL IA IB
MOV M4 OUT
----------------
```

(c)
```
----------------
MOV IA M2
MOV IB M3
MUL IA IB
MOV IA OUT
MOV IB M1
ADD IA IB
MOV M4 OUT
----------------
```

(d)
```
----------------
MOV IA M2
MOV IB M3
ADD IA IB
MOV IA OUT
MOV IB M1
MUL IA IB
MOV M4 OUT
----------------
```

(e) None of the above.

Question 3

With reference to the four-logic-gate as shown in Figure 1 in the lecture note "Processor and Computer", what is the truth table of the following logical operation?

$$Z = \neg A \oplus \neg B,$$

where $\neg A$ refers to the logical operation "NOT A" and $A \oplus B$ refers to the logical operation "XOR A B".

Answer:

A	B	$\neg A$	$\neg B$	Z
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	0

Question 4

With reference to the four-logic-gate as shown in Figure 1 in the lecture note "Processor and Computer", which of the following micro-program(s) can perform the logical operation.

$$Z = \neg A \oplus \neg B,$$

where $\neg A$ refers to the logical operation "NOT A" and $A \oplus B$ refers to the logical operation "XOR A B".

(i) 7-Step micro-program.

S1: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S2: $S_{14} = 01$ and $S_{15} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S3: $S_{13} = 01$ and $S_{12} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S4: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S5: $S_{14} = 01$ and $S_{13} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S6: $S_{15} = 01$ and $S_{12} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S7: $S_4 = S_7 = S_{11} = 1$. Other connectors and switches are set to 'Disconnection' mode.

(ii) 8-Step micro-program.

S1: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S2: $S_{14} = 01$ and $S_{16} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S3: $S_{13} = 01$ and $S_{12} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S4: $S_1 = S_8 = 1$. Other connectors and switches are set to 'Disconnection' mode.

S5: $S_{14} = 01$ and $S_{13} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S6: $S_{16} = 01$ and $S_{12} = 10$. Other connectors and switches are set to 'Disconnection' mode.

S7: $S_4 = S_7 = S_{11} = 1$. Other connectors and switches are set to 'Disconnection' mode.

S8: $S_{14} = 01$ and $S_{15} = 10$. Other connectors and switches are set to 'Disconnection' mode.

(iii) One-step micro-program.

S1: $S_4 = S_7 = S_{11} = 1$. Other connectors and switches are set to 'Disconnection' mode.

Answer: D.

(a) (i) and (ii).

(b) (ii) and (iii).

(c) (i) and (iii).

(d) (i), (ii) and (iii).

(e) None of the above.